CONSTRUCTIONAL NOTES

FOR THE SINGLE BOARD CONTROLLER CARD

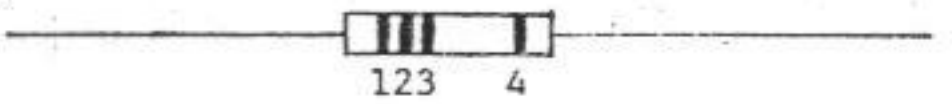
Component List and identification

I.C. sockets: 10 off 28 pins, 3 off 20 pins, 3 off 16 pins, 12 off 14 pins, 2 off 8 pins, 2 off 40 pins, and 4 off 20 way socket pin strips.

Resistors:

R1	220R	R9	470R
R2	220R	R10	10K
R3	4K7	R11	4K7
R4	1K	R12	4K7
R5	4K7	R13	470R
R6	120K	R14	4K7
R7	10K	R8	10K

Resistors are identified by their coloured bands which also serve to indicate their value. These bands are as shown:

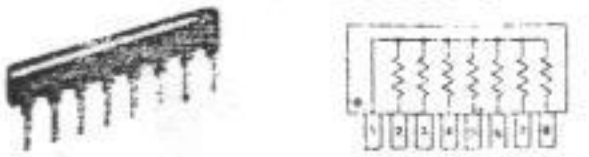


Ignore band 4 as this is irrelevant, it is only bands 1, 2 and 3 that are of interest. The colour code for R1 & R2 (220R) is:- red, red, brown; R3 (4K7) is:- yellow, mauve, red; and so on.....

S.I.L. resistor packages: These are also resistors, but are supplied in a ceramic film pack. Two types of S.I.L.s are used on this card, 7 commoned, which means 7 resistors all the same value, (usually marked on side of pack) with one end of each resistor connected together at pin 1, usually marked with a dot, and the other end of each resistor going to a separate pin. When fitting S.I.L.s, position the dot on the body at the same end as the dot on the P.C.B. legend.

RP1	4K7
RP4	1K

7-commoned resistors



The second type of S.I.L. used on this card is just a pack of 4 resistors each having separate pins.
These may be substituted for the normal type of resistors at the suppliers discretion.

RP2	10K
RP3	1K

4-individual resistors

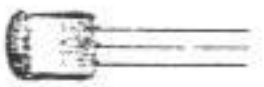
Capacitors:

C1	100n
C2	10n
C3	n10
C4	47n
C5	100mF 10v
C6	47n
C7-14	100n
C15	10n

Capacitors are identified by their values which are printed on them. They are usually small flat plates, rather than tubes and their leads are such that they stand up rather than lay down.

Transistors: There are three transistors, and these are identified by their three leads which are preformed triangularly.

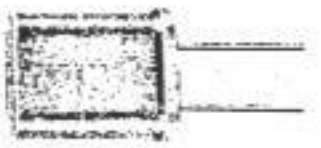
TR1-3 BC184



Links: LK1-25 are fitted with various lengths of pin strips, which are connected with shorting blocks. The shorting blocks are fitted in different positions, dependent on which processor option you decide on. For further link information see sheet marked "SYSTEM CONTROLLER LINKS".

Crystals: are easily identified as having a tin case and two wire legs at one end, the frequency is printed on the side or top.

XTAL1	8.0000 Mhz
XTAL2	1.8432 Mhz



Diodes: The diodes look a bit like resistors, they are usually black with a band at one end, and the type printed on them.
When fitting the diodes to the P.C.B. the band on the diode should be fitted facing the band on the legend to ensure correct polarity.

D1-3 1N4001

Terminal Block: 4 way P.C.B. mounting (Cass I/O)

Integrated Circuits:

B1	6522A	B2	6522A
C1	74LS393	C2	74LS04
C3	LM358N	D1	6551A
D2	(6502A) option	D3	(6809) option
D4	75150	E2	74LS244
E2	74LS244	F3	74LS139
G3	74LS00	H3	74LS266
J3	74LS12	K3	74LS10
* M3	74LS138 *	N3	(Map ROM) options
N2	74LS245	E1	Operating System

* Note:- I.C. M3 is fitted the other way round compared to the rest of the Integrated Circuits.

The remainder of the I.C. sockets can be fitted with either RAM, ROM or EPROM dependent on the mapping ROM chosen.

It should be obvious which devices are the integrated circuits, there isn't anything else left! They should be fitted into the I.C. sockets with pin 1 nearest to the dot on the printed circuit legend. The end of the integrated circuit with pin 1 has a pip or indentation dot next to pin 1 and/or a piece taken out of the moulding at pin 1 end.

For further constructional techniques and P.C.B. care, refer to Chapter Two of the Microtan 65 Manual.

SYSTEM CONTROLLER

*6502/6802/6808/6809 CPU.

*Fully buffered address, data, control buses.

*On-board 6/8 MHz clock, for .75, 1, 1.5, 2, 3 MHz operation - or by cutting one link - external clock.

*DMA Possible to all on-board devices.

*Low power.

*Fully decoded 1K memory mapped I/O space.

*Plugs into Tangerine system motherboard and is compatible with:

AIM TV Interface	(CPU clock = 1 MHz)
TANRAM	(CPU clock = $\leq$ 1 MHz)
32K RAM	(CPU clock = $\leq$ 1 MHz)
32K ROM/PROM	(CPU clock = $\leq$ 2 MHz)
High Res. Graphics	(CPU clock = .75 MHz)
TANDOS	(CPU clock = $\leq$ 1 MHz)
Parallel I/O	(CPU clock = $\leq$ 2 MHz)
Serial I/O	(CPU clock = $\leq$ 2 MHz)

*Up to two VIAs (6522s) to give

32 parallel I/O lines with handshake

4 sixteen bit programmable counter/timers

2 serial TTL data ports

Or

One VIA and one CIA (6526) to give all of the above (with more limited handshake but more versatile counter/timers) plus a set of time of day registers.

*RS232, 20 mA and TTL asynchronous serial interface (using 6551 UART).

*On-board I/O occupies 64 Bytes, positioned in the top 256 Bytes of I/O space according to 1 of 4 links.

*Lower cost replacement and improvement for Microtan/Tanex (except has no on-board VDU).

*Power on reset - an open-collector signal which is available at the I/O ports for use as an I/P or O/P.

*Software totally compatible with Microtan/Tanex.

*<u>Controller Memory</u>

1. 9 x 28 pin 27 series JEDEC sockets.
2. Each socket can be RAM/ROM/EPROM.
3. 2K/4K/8K Address space per socket (1K with rollover).
4. Maximum memory space = 64K.

5. Each socket is tailored to accept one of the above memory devices by means of a single jumper link.

6. Three different classes of socket on-board:

   A - 2 totally independant sockets (socket 0 and 1).

   B - 3 pairs of sockets (2 + 3, 4 + 5, 6 + 7) which must have the same class of chip in each one of the pair (or one can be empty).

   C - 1 socket (8) which can be any type of I.C. but will not recognise the BLOCK SELECT signal even when the rest of the board does. Typical use for this would be the monitor ROM or workspace RAM.

7. Each socket can be located anywhere in memory map in 2K steps (the paired sockets need not be contiguous).

   Alternatively, by swopping a board link the memory can be operated in page-select mode (2 pages) - enabling 1 of each pair of sockets and one of the two independant sockets in each page. (Socket 8 remains unaffected).

   It is thus possible to "swop" firmware packages residing in the same address space.

8. Enhances $\overline{\text{BLOCK ENABLE}}$ signal recognition - According to the state of two links, the $\overline{\text{BE}}$ signal from motherboard will affect either ROM only or RAM only or both (standard $\overline{\text{BE}}$ recognition) or neither.

   NB: $\overline{\text{BE}}$ affects only memory not the processor or I/O (or socket 8).

9. Removing 4 I/Cs plus processor turns the board into a memory board driven via TANBUS (by Microtan/Tanex or another controller card), losing none of the RAM/ROM/IO versatility described above.

10. The memory address map is defined by a bi-polar prom. Three options are available to the user:

    Standard address map prom. - similar to Microtan/Tanex, i.e. 8K RAM, 16K PROM.

    Custom prom. - blown to user specifications.

    Optional bi-polar prom. programmer - plugs into one I/O port and supplied complete with firmware driver.

11. When using a 6802, the on-chip RAM can be utilised in a prom-based system. This RAM is enabled by a link, after which socket 0 should be left unused.

SYSTEM CONTROLLER LINKS

Issue 2

LK1 6802 Ram Enable Link

For a 6802, link common to A to enable on-chip RAM, common to B to disable. For all other µps, link to A.

LK2 65/68 Clock Select

For 6502 - Comm to B

6802
6808 - Comm to A
6809

LK3 Clock Speed Select

For 68 series with 8 MHz XTAL, jump LK3 for 2 MHz operation.
jump LK4 for 1 MHz operation.

For 6502 with 6 MHz XTAL, jump LK5 for 1.5 MHz operation.
jump LK6 for 0.75 MHz operation.

For 6502 with 8 MHz XTAL, jump LK5 for 2 MHz operation.
jump LK6 for 1 MHz operation.

N.B. Only one link to be made at any one time.

LK7 External Clock Link

Normally made - remove jump link if external clock is required (from edge connector)

LK8 Cassette Link

Normally made - remove jump link to totally disable cassette input.

N.B. Under normal use - cassette will not affect the I/P port unless the cassette recorder is playing.

LK9 Standby +5

Normally made - when using 6802 if jump link removed Pin A can be connected to a separate +5 supply to provide a low power data retention mode; retaining the first 32 bytes of on-chip RAM.

LK10	I/O Position Select	LK10 enables on-board I/O in the top 64 bytes of I/O space.
LK11		LK11 - second 64 bytes of I/O.
LK12		LK12 - third 64 bytes of I/O.
LK13		LK13 - fourth 64 bytes of I/O.
LK14	Memory Links	Define the memory socket.
15		X linked to A
16		4K x 8 PROMS
17		8K x 8 PROMS
18		4K x 8 RAMS
19		8K x 8 RAMS
		X linked to B
		1K x 8 RAMS
		2K x 8 RAMS
		X linked to C
		2K x 8 PROM

In the case of links 14, 18 and 19 the link defines only the socket immediately adjacent (i.e. Ø, 7 and 8).

However, link 15 defines both socket 1 and 2
16 3 and 4
17 5 and 6

LK20	DMA Link	Normally made.
LK21	ROM Enable Link	Common to B enables Block Enable signal from edge connector to disable ROM memory space on board (except for a ROM in socket 8). Common to A disables this facility.
LK22	RAM Enable Link	As LK21
LK23	Pseudo-static RAM Link	PCB made link. If Pseudo-static RAMs are used the PCB link should be broken and an external circuit linked to pad A to drive the refresh pin.
LK24	Page Select Link	Normally common linked to A. If linked to B an output port line drives part of the memory decoding circuit enabling 2 separate pages of memory to be present, occupying to same address space.

LK25	6526 Select Link	Normally made if a 6526 is used in socket B2 the link can be broken and pad A connected to a 50 Hz TTL compatable signal to drive its Time of Day registers. This signal can either be the TANBUS FB (Field Blanking) signal, taken off the edge connector and available on the System Controller, or (if greater accuracy is required) an externally generated signal.

SYSTEM CONTROLLER IC POPULATION

Processor Card

6502, 6802, 6808 } Are fitted in D3

6809 ls fitted in D2

Memory Card

E2, E2, C1, L3, G3 are left off when the board is operated as a memory - I/O card.