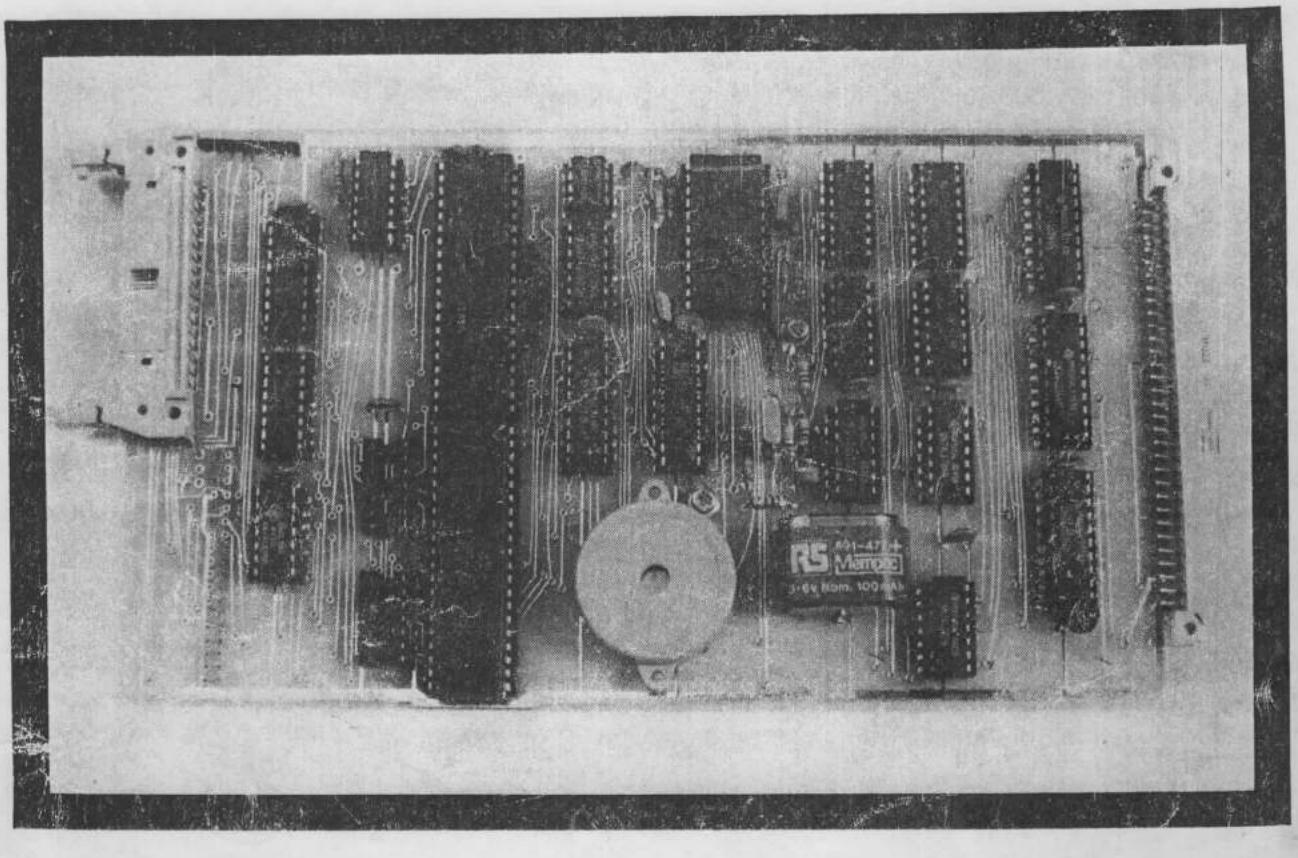
Ralph Allen Engineering Co.

FORNCETT END NORWICH
NORFOLK ENGLAND
Reg. No. 1711588 *TEL: BUNWELL (095389) 420* V.A.T. No. 353 2120 00

* * DISC CONTROLLER CARD * *



This disc controller card uses the same 1793/9216 controller chips as the origanal Tangerine card does to help keep the upgrade as cheap as possible but there the similarity ends, this card is intended for use with our 6809 Flex system, although it can be used in a 6502 in conjunction with our 32K ram/eprom card as the disc card has no on-board memory or eprom as does the origanal Tangerine card.

This card is capable of controlling four 40/80 single or double sided 5 1/4" floppy disc drives single or double density, in addition it has a real time clock that is battery backed and that can answer the date prompt when booting flex, this also has 30 bytes of battery backed ram built in that could be used for retaining system or program details on power down. additionally there is also a bleeper that can draw your attention to system or program errors and this will be utilized in our next 6809 monitors, and a 6522 VIA that can be used to drive a printer or plotter.

PRICE £24.50p BARE P.C.B. + VAT and £1.50p postage.

PLEASE PHONE FOR BUILT AND TEST PRICES.

DOS/RTC
COMPONENT LIST

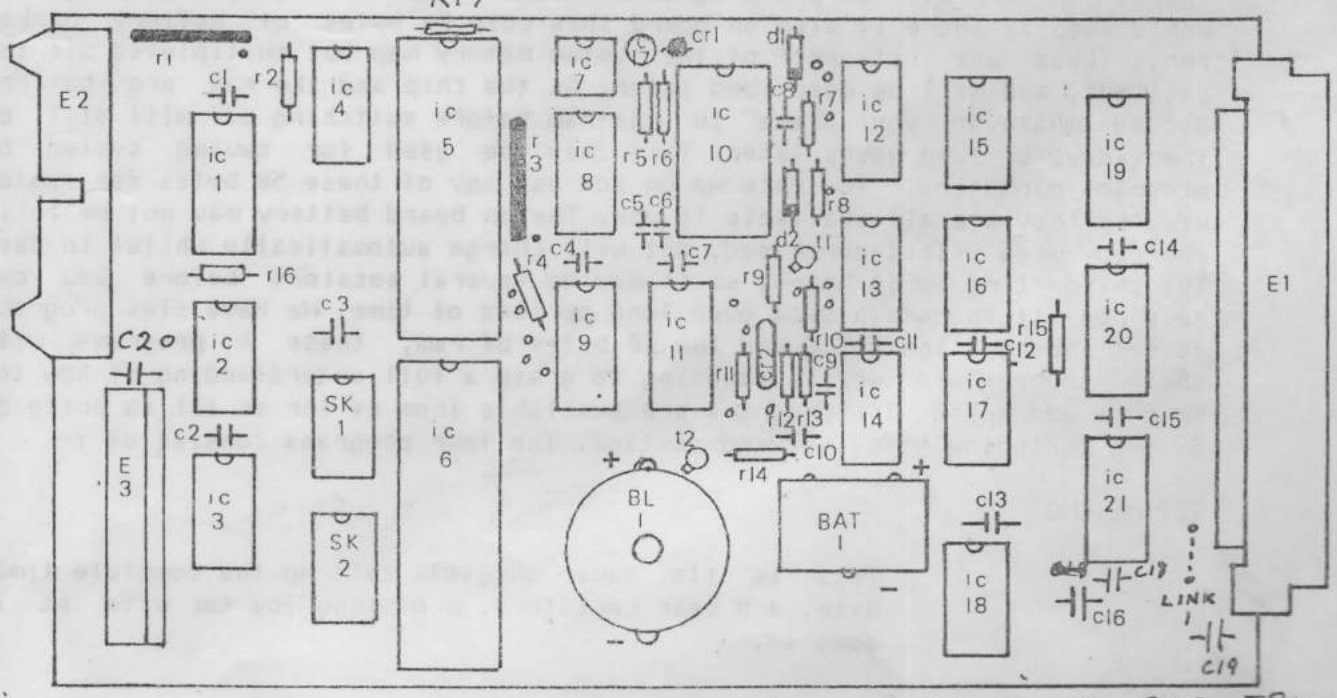
IC1	74LS642-1 must be -1
IC2	74156
IC3	74LS00
IC4	74LS21
IC5	1793 or 8877 FDC
IC6	6522 VIA
IC7	WD9216 CA00 or 01
IC8	74LS393
IC9	74LS273
IC10	CDP6818E or 146818
IC11	74LS244
IC12	74LS139
IC13	74LS21
IC14	74LS04
IC15	74LS138
IC16	74LS32
IC17	74LS73
IC18	74LS02
IC19	74LS244
IC20	74LS244
IC21	74LS245
BAT1	RS591-477 3.6V 100mah
BL1	Vero Speed 41-22514C Bleeper Passive
T1,2	BC109
CR1	32.768 KHZ Crystal
CR2	4 MHZ Crystal

1 off	8 pin Dil socket
10 off	14 pin Dil socket
3 off	16 pin Dil socket
6 off	20 pin Dil socket
1 off	24 pin Dil socket
2 off	40 pin Dil socket

R1	150R X 7 SIL
R2	1K
R3	4K7 X 7 SIL
R4	1K
R5	150K
R6	4M7
R7	2K
R8	470R
R9	1M
R10	1K
R11	12K
R12	1K
R13	1K
R14	1K
R15	300R
R16	1K
C1-4,7	.1uf ceramic
C5,6	33pf ceramic
C8	4n7 ceramic
C9	10n ceramic
C10	n10 ceramic
C11-15	.1uf ceramic
C16	n12 ceramic
C17	0-20 pf varible
C18	47uf Tantalum
E1	64/64 Edge connector Vero
E2	34 Disc drive connector
E3	25 Way D Type RS-466-220
SK1,2	14 Pin Output socket
D1,2	OA91 diode
LINK 1	Insert to enable interrupts from RTC
C19	10uf TANT 16v
C20	10uf TANT

R17 ← R17 12K

WE STOCK ALL OF THE ABOVE PARTS SHOULD YOU HAVE ANY TROUBLE OBTAINING THEM.



ADD A LINK TO GND FROM PIN 20 of IC10

DOS/RTC DESCRIPTION

This card has been especially developed for our 6809 Flex system. However, it will funtion in a 6502 system if used with one of our 32K Eprom Ram cards to hold the Eproms that would normally fit on the original Tangerine board.

The board is made up of four different sections, these are :-

1 Disc Controller section, to control four, forty or eighty track, single or double sided drives, single or double density.

2 A Real Time Clock with interrupt capabilities, together with 50 bytes of battery backed Ram.

3 An onboard Bleeper to draw your attention to the terminal when a program error occurs, and which can also be used as a Keypress bleeper.

4 A 6522 VIA which can be used to drive a plotter or printer.

Taking the sections in the above order :-

* * * DISC DRIVE CONTROLLER SECTION * * *

The floppy disc controller chip is addressed in the same location and manner as was the one on the original Tangerine. This was necessary to maintain compatibility with our Flex that was originally done to run on the Tangerine board. The Disc control and status register is located at $BF90, the track register at $BF91, the sector register at $BF92, and the data register at $BF93, followed by the board register at $BF94. There is no need for you to use any of these registers or to be concerned with them in any way whatsoever, as they are handled totally from within the disc drives routines embedded into your Flex. For those of you who may like to know how it all works we suggest that you obtain a data sheet on the 1793 FDC chip.

* * * REAL TIME CLOCK * * *

The real time clock chip, for those of you not familiar with them, is simply as its name suggests, a clock to tell the time of day. The ability of this chip to cause interrupts by the second, minute, or hour makes it invaluable for allowing your computer to be able to control the real world by switching things on or off at pre-programmed times of day or night, or timing real world events. There is also on board this chip 50 bytes of battery backed ram. These are not part of the system memory map but multiplexed off the data bus, and will be described later. As the chip and the ram are battery backed whatever you place in the ram before switching off will still be there days or even weeks later. This may be used for saving system or program parmeters. To date we do not use any of these 50 bytes for system use, so they are all available to you. The on board battery may not be fully charged when first purchased, but will charge automatically whilst in use. The charge time is 14 hours, so it may be several sessions before you can rely on it to retain data over long periods of time. We have flex programs to set and read the R.T.C and the 50 bytes of ram, these 4 programs with their source are worth studying to grasp a full understanding of how the chip is addressed. The programs are available from us for an all in price of £7.50p including disc, vat and postage. The four programs consist of :-

SETIME.CMD

This as its name suggests sets up the complete time, date, and year registers, prompting you for data as it does so.

TIME.CMD

Simple reads the time, day and date and displays them to the screen as:-

The time is 10.20am & 5 seconds Friday the 16th September 1985.

RTCSET.CMD

This allows manual setting of any of the time or ram locations, and can also be usd to reset just the minutes or seconds register if you clock goes out, this save having to reset all of the time and date registers when only one is wrong.

RTCREAD.CMD

Reads all 64 byte locations and displays them as a hex dump.

The above programs will only work with our V1.2 or later monitors.

For those of you that require a full understanding of the R.T.C. chip we can supply data sheets at $1.80p a set plus 20p postage. These consist of 18 pages of A4.

For those of you not wishing to study it to that depth a brief description follows.

The chip occupies only two memory locations within the memory map of the system; they are $BF98 and $BF99, the first address being the address register and the second the data register. The first 14 locations within the chip are for the time portion of the R.T.C and we will come back to them later. Starting from location $0E hex, ie the 15th byte, (the first byte is 0) you can store data into this location by first sending the address of the byte that you wish to access ($0E in this case) to the address register, followed by the data that you wish to place in it to the data register.

Example :-

```
LDA £$0E(ADDRESS OF INTERNAL BYTE
STA $BF98 THE ADDRESS REGISTER
LDA £$FF THE DATA YOU WISH TO STORE
STA $BF99 THE DATA REGISTER
```

TO READ FROM AN INTERNIL(REGISTER YOU NEED

```
LDA £$0E THE ADDRESS OF THE BYTE THAT YOU REQUIRE
STA $BF98 SEND TO ADDRESS REGISTER
LDA $BF99 THE CONTENTS OF $0E ARE NOW IN THE 'A'
          REGISTER
```

Note these commands must come from within a program and not using the monitor MEM command as this reads a location before writing to it.

The time registers are as follows:-

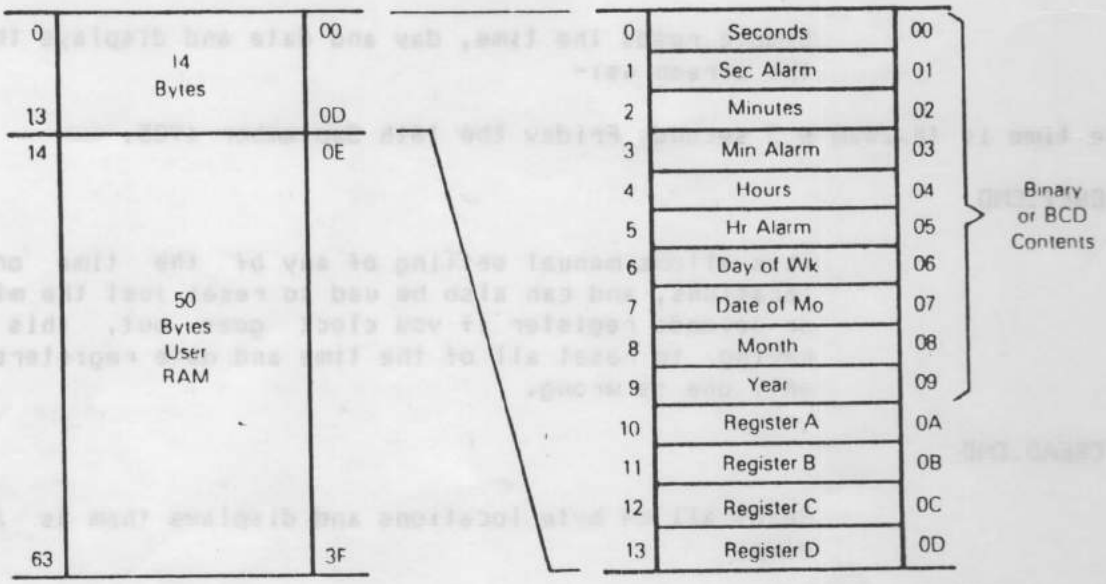


TABLE 3 – TIME, CALENDAR, AND ALARM DATA MODES

Address Location	Function	Decimal Range	Range		Example*	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0	Seconds	0-59	$00-$3B	$00-$59	15	21
1	Seconds Alarm	0-59	$00-$3B	$00-$59	15	21
2	Minutes	0-59	$00-$3B	$00-$59	3A	58
3	Minutes Alarm	0-59	$00-$3B	$00-$59	3A	58
4	Hours (12 Hour Mode)	1-12	$01-10C (AM) and $81-$8C (PM)	$01-$12 (AM) and $81-$92 (PM)	05	05
	Hours (24 Hour Mode)	0-23	$00-$17	$00-$23	05	05
5	Hours Alarm (12 Hour Mode)	1-12	$01-$0C (AM) and $81-$8C (PM)	$01-$12 (AM) and $81-$92 (PM)	05	05
	Hours Alarm (24 Hour Mode)	0-23	$00-$17	$00-23	05	05
6	Day of the Week Sunday = 1	1-7	$01-$07	$01-$07	05	05
7	Day of the Month	1-31	$01-$1F	$01-$31	0F	15
8	Month	1-12	$01-$0C	$01-$12	02	02
9	Year	0-99	$00-$63	$00-$99	4F	79

*Example: 5:58:21 Thursday February 1979

Below these are the control registers as described by this section of the data sheet that follows.

REGISTERS

The CDP6818 has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

REGISTER A ($0A)

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0	Read/Write
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Register except UIP

UIP – The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244 µs (for all time bases). This is detailed in Table 6. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero – it is not in transition. The UIP bit is a read-only bit, and is not affected by Reset. Writing the SET bit in Register B to a "1" inhibit any update cycle and then clear the UIP status bit.

TABLE 6 – UPDATE CYCLE TIMES

UIP Bit	Time Base (OSC1)	Update Cycle Time (t_{UC})	Minimum Time Before Update Cycle (t_{BUC})
1	4.194304 MHz	248 µs	–
1	1.048576 MHz	248 µs	–
1	32.768 kHz	1984 µs	–
0	4.194304 MHz	–	244 µs
0	1.048576 MHz	–	244 µs
0	32.768 kHz	–	244 µs

DV2, DV1, DV0 – Three bits are used to permit the program to select various conditions of the 22-stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use. Table 4 shows that time bases of 4.194304 MHz, 1.048576 MHz, and 32.768 kHz may be used. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider at the precise time stored in the RAM. When the divider reset is removed the first update cycle begins one second later. These three read/write bits are never modified by the RTC and are not affected by $\overline{\text{RESET}}$.

RS3, RS2, RS1, RS0 – The four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tape selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The program may do one of the following: 1) enable the interrupt with the PIE bit, 2) enable the SQW output pin with the SQWE bit, 3) enable both at the same time at the same rate, or 4) enable neither. Table 5 lists the periodic interrupt rates and the square-wave frequencies that may be chosen with the RS bits. These four bits are read/write bits which are not affected by $\overline{\text{RESET}}$ and are never changed by the RTC.

REGISTER B ($0B)

MSB							LSB	
b7	b6	b5	b4	b3	b2	b1	b0	Read/Write Register
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	

SET – When the SET bit is a "0", the update cycle functions normally by advancing the counts once per second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is read/write bit which is not modified but $\overline{\text{RESET}}$ or internal functions of the CDP6818.

PIE – The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit to cause the $\overline{\text{IRQ}}$ pin to be driven low. A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Control Register A. A zero in PIE blocks $\overline{\text{IRQ}}$ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal CDP6818 functions, but is cleared to "0" by a $\overline{\text{RESET}}$.

AIE – The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to "0". The internal functions do not affect the AIE bit.

UIE – The UIE (update-ended interrupt enable) bit is a read/write bit which enables the update-end flage (UF) bit to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears the UIE bit.

SQWE – When the square-wave enable (SQWE) bit is set to a "1" by the program, a square-wave signal at the frequency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a zero the SQW pin is held low. The state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. SQWE is a read/write bit.

DM – The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or $\overline{\text{RESET}}$. A "1" in DM signifies binary data, while a "0" in DM specifies binary-coded-decimal (BCD) data.

24/12 – The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a "0"). This is a read/write bit, which is affected only by the software.

DSE – The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1"). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or $\overline{\text{RESET}}$.

REGISTER C ($0C)

MSB							LSB	
b7	b6	b5	b4	b3	b	b1	b0	Read-Only Register
IRQF	PF	AF	UF	0	0	0	0	

IRQF – The interrupt request flag (IRQF) is set to a "1" when one or more of the following are true:

PF = PIE = "1"

AF = AIE = "1"

UF = UIE = "1"

i.e., IRQF = PF•PIE + AF•AIE + UF•UIE

Any time the IRQF bit is a "1", the $\overline{\text{IRQ}}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{\text{RESET}}$ pin is low. A program write to Status Register 2 does not modify any of the flag bits.

PF – The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an $\overline{\text{IRQ}}$ signal and the IRQF bit when PIE is also a "1." The PF bit is cleared by a $\overline{\text{RESET}}$ or a software read of Register C.

AF – A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the $\overline{\text{IRQ}}$ pin to go low, and a "1" to appear in the IRQF bit, when the AIE bit also is a "1." A $\overline{\text{RESET}}$ or a read of Register C clears AF.

UF – The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting $\overline{\text{IRQ}}$. UF is cleared by a Register C read or a $\overline{\text{RESET}}$.

b3 TO b0 – The unused bits of Status Register 1 are read as "0's". They can not be written.

REGISTER D ($0D)

MSB							LSB	
b7	b6	b5	b4	b3	b2	b1	b0	Read Only
VRT	0	0	0	0	0	0	0	Register

VRT – The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power-sense pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read/only bit which is not modified by the $\overline{\text{RESET}}$ pin. The VRT bit can only be set by reading the Register D.

b6 TO b0 – The remaining bits of Register D are unused. They cannot be written, but are always read as "0's."

As stated previously for a full understanding you will need the complete set of data sheets.

INTERRUPTS:- To enable the interrupts from the RTC, insert LINK 1 as shown in the board layout diagram. This connects the 'interrupt' output of the RTC chip to the IRQ line on the Tangerine bus. On Issue 2 CPU cards this line is connected to the IRQ pin on the 6909 microprocessor. Owners of Issue 1 cards will simply need to strap pin 3 of the 6809 microprocessor socket to pin A14 on the CPU card edge connector.

* * * BLEEPER * * *

This on board bleeper is addressed by writing to $BF95, and funtions as a toggle ie:-

STA $BF95 will turn it on.

STA $BF95 will turn it off.

The contents of tha 'A' register is irrelevant, just the act of writing to that address activates it.

As a demo try :-

MEM BF95 xx 00 the xx are the values returned by the monitor.

When you enter 00 or any other hex characters that the monitor will accept, you have just written to $BF95 and the bleeper will switch on. Now press ESC so that the monitor is again showing $BF95 and now enter two more digits and the bleeper will switch off. If you have the V1.2 or later version of our monitors the BLE command will cause a bleep every time you press a key. Also any program that sends an $07 error code will also sound the bleeper to draw your attention to the error. For those of you using ED3 re-run CONGEN and enter $07 where it asks for bell code. You will also find that $BF97 will activate the bleeper but don't use this address as it also phantoms onto the disc driver registers.

* * * VERSATILE INTERFACE ADAPTOR * * *

This on board VIA can be used to drive a printer or plotter or anything else of your choice. It is addressed from $BF80 to $BF8F and the VIA registers are as shown in the following table. If you wish to use this port to drive

your printer that you may currently have plugged into Tanex you will need to change your PRINT.SYS file to these new addresses. This is done by replacing all of the address in the source code supplied on your master Flex disc from $BFEx to $BF8x, the x remains at its original value. Having done this re-assemble and call the resulting binary file PRINT.SYS. The 2 sockets next to the VIA chip are tracked in the same way as the printer sockets on Tanex so by taking the printer header plug from socket C1 on tanex and placing it into socket SK1 and the printer header from D1 on Tanex and placing into socket SK2 on the DOS/RTC, your Flex and printer will now work from the new DOS/RTC card the same as they did from Tanex. You will need to reboot or GET 0.PRINT.SYS to load the new PRINT.SYS into memory.

SOCKET DETAILS

Pin No	SK1	SK2	Signal Direction
1	+5V	+5V	-
2	PA0	PB0	In/Out
3	PA1	PB1	In/Out
4	PA2	PB2	In/Out
5	PA3	PB3	In/Out
6	PA4	PB4	In/Out
7	ground	ground	-
8	ground	ground	-
9	PA5	PB5	In/Out
10	PA6	PB6	In/Out
11	PA7	PB7	In/Out
12	CA2	CB2	In Only
13	CA1	CB1	In/Out
14	+5V	+5V	-

CONNECTIONS TO E3 ARE :-

Pin No		Pin No	
1	ground	13	+5V
2	PB5	14	ground
3	PB6	15	PB4
4	PB7	16	PB3
5	CB2	17	PB2
6	CB1	18	PB1
7	N/C	19	PB0
8	PA5	20	PA4
9	PA6	21	PA3
10	PA7	22	PA2
11	CA2	23	PA1
12	CA1	24	PA0
		25	+5V

N/C = Not Connected.

Note :- To be able to fit E3 you will have to use the smaller type of edge connector for E1 (The type without locking lugs)

The following information gives a full description of the 6522 VIA.

Reference to registers 1,5,15 etc, are indexed addresses from the VIAs base address of $BF80, i.e. register 1 is at $BF81, 5 at $BF85, 15 at $BF8F etc.