* * * * * * * SETTING UP * * * * * * *

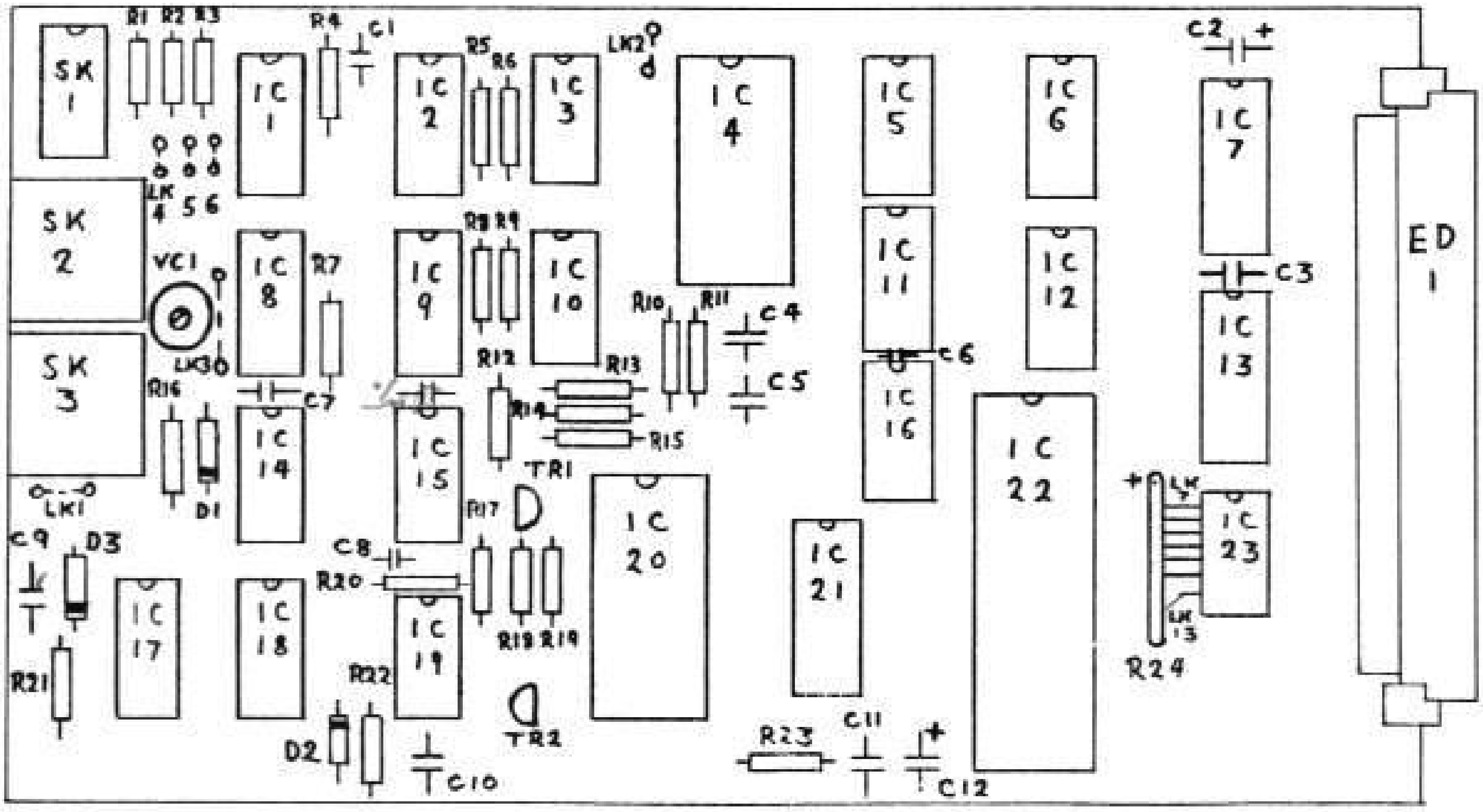
The, only setting up required for this card, is to very carefully adjust the variable capacitor VR1 until all the characters are visible. If you are using this card in a system other than our own, you will need to study the RALBUG monitor source code, available from us. See address at rear of this manual.

If using a Tangerine system with our 6809 conversion, place the card into any additional slot, or any slot if using our Micro-set system.

Having done the above press reset and the screen should become steady, probably filled with shimmering rectangular blocks. At the lower left corner of the screen will be our RALBUG Vx.x header, although this may not as such be readable. You may have every other letter missing, or possibly nothing at all. Now very carefully and slowly turn the varible capacitor until the letters all appear and become steady, when you have a good display enter the monitor ASC command and fine tune the capacitor with a screen full of text. You should be able to obtain a perfect display, if the edges of some of the characters are shimmering then you do not have the tuning quite right.

You may find when the board is new you may have to retune the first two or three times you use the system, or the characters may shimmer when the board is warming up. This will disappear after about three days and no more tuning will be required. If you are unable to make the board funtion you may return it to us for repair, this is a fixed charge of £25 plus vat and postage.

2. IC1 ?
3. tracks on CPU ?
4. trimmer; value of cap



20pF

LS367

--- COMPONENT LIST ---

IC1	8T97
IC2	74LS221
IC3	74LS86
IC4	6116LP3 ram
IC5	74LS30
IC6	74LS157
IC7	74LS244
IC8	74LS132
IC9	74LS32
IC10	74LS86
IC11	74LS138
IC12	74LS157
IC13	74LS244
IC14	74LS86
IC15	74LS00
IC16	74LS157
IC17	74LS174
IC18	74LS174
IC19	74LS20
IC20	SAA5055 see note
IC21	74LS245
IC22	6845
IC23	74LS30

R1-3	220R
R4-5	5K6
R6	39K
R7	510R
R8	10K
R9	22K
R10	680R
R11	1K
R12	10K
R13-16	5K6
R17	1K
R18-19	100R
R20	4K7
R21	220R
R22	5K6
R23	220R
R24	10K X 8 SIL
C1	47p
C2	47uf Tant
C3	.1uf
C4	120p
C5-7	.1uf
C8-9	22n

C10	470p
C11	120p
C12	10uf Tant
D1-2	IN1418
D3	5v1 Zenor
VC1	0to20pf ver cap
SK1	14 pin dil socket
SK2-3	5 pin din (maplin) part No YX91Y
ED1	96/96 or 64/64 edge connector (see text)

We stock the full range of components for our boards should you be unable to obtain any part.

TR1	BC550 or 547
TR2	BC184L MUST BE L

14 PIN dil sockets 10 off
16 PIN dil sockets 8 off
20 PIN dil sockets 3 off
24 pin dil socket 1 off
28 pin dil socket 1 off
40 pin dil socket 1 off

Note SAA5055 will give you true ASCII, we some times have these in stock but they are expensive. You can use the SAA5050 which is much cheaper and easily obtained from most chip stockist, but it is teletex characters, it lacks [{}] and a few others. The 5055 is a must for 'C' programming.

COLOUR VIDEO ISSUE 1

This Video card is intended for use within our own 6809/68008/68000 rack system but may equally well be used with any other system that can supply the required bus signals, see section on bus pins used. The card will supply 81 characters by 25 lines of steady flicker free video and 162 x 75 pixcel graphics. Eight colours can be displayed for R.G.B colour monitors, or 8 grey levels for composite monochrome video. Memory mapped to $E000-$E7FF it contains its own on board video ram and has a programmable cursor. If you intend fitting this card in another system, see section at rear.

* * * INSTALLATIONS * * *

The card plugs into any slot of our 96/96 back bus, or, any of the additional slots in a Tangerine system fitted with our 6809 conversion. We advise Tangerine owners to build this card using the 96/96 way edge connector, then if you update later to our 6809/68000 bus you will not have to cut the side off the edge connector to be able to use this card. The software to drive it is contained within our RALBUG monitors current version V1.3, earlier versions had the card mapped to a different memory location. If you are trying to install this card in another system the source code is available for the V1.3 monitor at £5 per print out. If used in our system there will be no memory contention problems, as the video card disables system ram which conflicts with its own address map. Other systems will have to disable or remove the contending ram.

DISPLAY DATA

The screen is mapped from $E000 to $E7FF. $E000 being the top left hand corner of the display, the next line down is 81 decimal 51 Hex from this address, example:-

$E000.....$E050
$E051 $E0A1
$E0A2.....$E0F2
$E0F3 $E143
$E144.....$E194
$E195 $E1E5
$E1E6.....$E236
$E237 $E287
$E288.....$E2D8
$E2D9 $E329
$E32A.....$E37A
$E37B $E3CB
$E3CC.....$E41C
$E41D $E46D
$E46E.....$E4BE
$E4BF $E50F
$E510.....$E560
$E561 $E5B1
$E5B2.....$E602
$E603 $E653
$E654.....$E6A4
$E6A5 $E6F5
$E6F6.....$E746
$E747 $E797
$E798.....$E7E8

The 6845 chip that controls this card has 15 registers that control the display. We do not recommend that you attempt to change these as they are set up by the monitor eprom at RESET. But for completeness we will list them below. To obtain access to these registers you must write the register address that you wish to access, offset from a base address of zero, into location $E7FE followed DIRECTLY by the data you wish to store in that register sent to $E7FF, see our monitor source code for a better understanding. Note. this can not be done using our Monitor Memory modify command.

Registers 0 to 3 are the horizontal timing registers and must not be changed in any way. If your video display area is not central to your screen this can be altered by changing register 2. You will have to consult our source printout and the full data sheet of the 6845 chip to be able to do this.

Registers 4 to 9 are the vertical timing registers and again should not be touched. The displayed area can be moved vertically by consulting the source code print out and a data sheet.

Register 10 (decimal)

This is a 7 bit write only register that controls the cursor format. Bit 5 of this register is the blink timing control, if high the blink rate is 1/6 of the vertical field rate, if low 1/32. Bit 6 is used to enable a blink. The cursor start scan line is set by the lower 5 bits.

Example :-

Bit 6	Bit 5	Cursor effect
0	0	Non blinking
0	1	Not visible
1	0	Fast blink
1	1	Slow blink

Register 11 (decimal)

This is a 5 bit write-only register which sets the cursor end scan line.

Register 12 & 13

Start address register, is a 14 bit register write-only register which determines the first address put out as a refresh address after vertical blanking. It consists of an 8 bit lower and 6 bit higher register.

Register 14 & 15

This is a cursor register, it is a 14 bit read/write register that stores the cursor location. This register consists of an 8 bit lower and 6 bit higher address. It should not be used by the user as RALBUG has full control over it.

Register 16 & 17

These are light pen registers, they are not used on this issue 1 card.

* * * * * * * DISPLAY GENERATION * * * * * * *

The display for this card is generated by a SAA5055 chip which will give you 6 colours plus black and white, this applies to the characters and the background colour; ie you have 8 foreground and 8 background colours. These are set to green characters on a black background by RALBUG V1.3 but can easily be changed by refering to the source code print out, or using the COL command from within RALBUG. Normal characters are displayed by storing their ASCII binary number into the video byte at the location that you wish them to appear. It is possible to change colour anywhere within a text line by simply storing a colour code (see table later) at the position where you wish the colour to change, this will leave a space in the text line. The same is true for the flash and and steady codes. By setting the 8th bit of any ascii character,that character will be displayed in inverse video.

COLOUR CONTROL CODES

The codes listed below are the codes that you would store directly into the screens video memory. If you are sending the character via SK-DOS, FLEX or our monitor display routines you will have to use different numbers to prevent clashing with system control codes, see source print out for details. The above is also true if sending CHR$() from within a basic program. All the FOURTH languages we supply have this taken into consideration, and the colour WORDS are available for your immediate use.

CONTROL	FUNCTION	HEX	DECIMAL
Alphanumeric	Red	$01	1
"	Green	$02	2
"	Yellow	$03	3
"	Blue	$04	4
"	Magenta	$05	5
"	Cyan	$06	6
"	White	$07	7
FLASH		$08	8
STEADY		$09	9
GRAPHIC	Red	$11	17
"	Green	$12	18
"	Yellow	$13	19
"	Blue	$14	20
"	Magenta	$15	21
"	Cyan	$16	22
"	White	$17	23
CONCEAL DISPLAY		$18	24
CONTINUOUS GRAPHICS		$19	25
separate GRAPHICS		$1A	26
BLACK BACKGROUND		$1C	28
NEW BACKGROUND		$1D	29
HOLD GRAPHICS		$1E	30
RELEASE GRAPHICS		$1F	31

Graphic characters are made up of 6 blocks per ASCII character. Two across by three deep. There are two types, separate blocks, or continuous blocks; ie blocks with gaps between them or blocks that touch to form solid blocks of colour. The type required is selected using the continuous graphic code $19 hex or the separate graphic code $1A hex. The separate code generates a small blank boarder around each graphic pixcel. As stated earlier control codes leave a space within a text line, the same is true of a graphic block. However there is a code listed as HOLD GRAPHICS, if this code is placed into a line it will make the graphics character previous to the space repeat over the control code hence closing the gap in the line. The release character code nullifies the above.

The graphic character is made up of Two blocks across by Three down to every ASCII character cell.
As shown:-

```
* *
* *
* *
```

The bit numbers to activate the cells are as follows:-

```
0 1          1 2
2 3          4 8
4 6   HEX   16 64   DECIMAL
```

Note. bit 5 must always be a '1' for graphics characters. This allows you to mix graphics and upper case characters on the same line without having to put in control codes.

If you wish to illuminate a group of pixels within the same ASCII character cell just add these values together and add 32 to the total, then poke this value to the screen location.

* * * * * * * OUTPUT SOCKETS * * * * * * *

SOCKET 1

External videoInput *** output socket

Pin details are:-

Pin	1	composite sync output @ 5 volts
Pin	2	N/C
Pin	3	Horizontal blanking output
Pin	4	Red input
Pin	5	Blue input
Pin	6	Green input
Pin	7	Ground
Pin	8	Blue output
Pin	9	Green output
Pin	10	Red output
Pin	11-13	N/C
Pin	14	VCC

These pin outputs are compatible with earlier cards that were on the market. If inputting video to this card Links 4 5 6 must have their tracks cut, there are pads available for rejoining them at a later date if you so wish. To bring in Monochrome video feed into pins 4,5 & 6 together.

SOCKET 2

R.G.B. output.

Pin

1 composite sync.
2 Ground
3 Red. T.T.L
4 Blue T.T.L
5 Green T.T.L

The R.G.B colour monitor output (Socket 2 upper socket) is set to give T.T.L output with negative sync, this can be changed to positive by cutting the track at link 1. Pads are there to enable you to re-make this link later should the need arise.

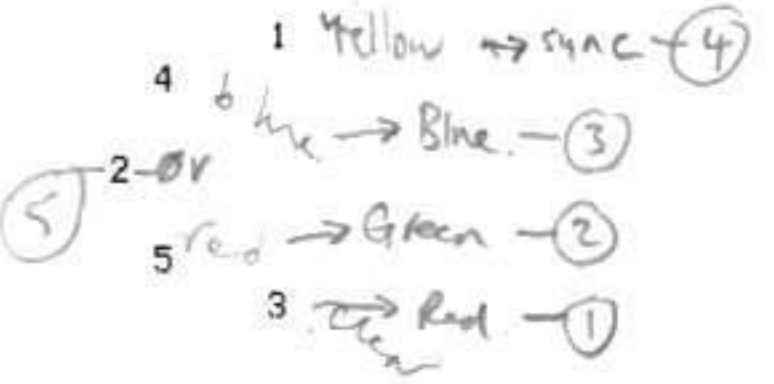
SOCKET 3

Monochrome. 1V P/P 75 ohms

Pins
1,3,4,5 video out
2, ground

The monochrome output socket (Socket 3 the lower one) is set to give 1v peak to peak composite sync video into 75 ohms.

DIN Pin numbering looking into socket.



* * * * * * * LINK DETAILS * * * * * * *

The card as tracked is set to give a non interlaced display, that is 312 lines per 20ms frame. As supplied no links need be made or broken if this card is being used in one of our systems, and it will be the only video used.

Link 1 if broken will supply a POSITIVE sync signal to the R.G.B output socket, socket 2.

Links 2 & 3 respectivlyeyely are to enable the vertical and horizontal syncs to be connected to the back bus (Note. if using this card with our 6809 Tangerine conversion you must cut the tracks supplying opposing vertical and horizontal sync coming from the CPU card). The purpose of joining these sync signals to the back bus is to lock in another video card, if this is the only video card in the system these links should remain broken. Another video card can be brought into this card via socket 1, the 14 pin socket at the top left of the card.

There are 3 links behind socket 2, these links are supplied tied to ground and only need to be broken if you intend bringing in an external video source, the source would be fed into socket 1 as described in the SOCKET detail section. When feeding in external video the appropriate links 4,5,& 6 need to be cut to allow the input signals to function. Link 4 is connected to pin 6 of socket 1. Link 5 to pin 5 and link 6 to pin 4. Link 4 is the green input link 5 is blue and link 6 is red. If you later remove the external video source you must re-make these links, there are pads on the card for this purpose

This card has been made to be able to reside in our 68000 system, and has the full 24 address lines decoded. As supplied it will work in our 6809 Tangerine conversion as described in this manual, however there are links on the card marked 7 to 14 which are connected to the 'C' row of the 96/96 edge connector, by cutting 1 or more of these links the card will move its address map up into higher memory ie $FFE000. Please note the card will work in a 6809 system with either the 64/64 or 96/96 edge connector fitted.

* * * * * * * BUS PINS USED BY THIS CARD * * * * * * *

Customers wishing to use this card in a system other than our own should note that there is a pin used on the edge connector (pin No A28) that is an output signal from this card, its purpose is to disable ram in the main system memory and prevent it clashing with this cards address map.

The MICRO-SET back bus connections are as follows :- (at 2/7/86)

c	b	a	
+5v	+5v	+5v	1
N/D	CLK	N/D	2
N/D	01	E	3
N/D	RST	I/O	4
A16	A1	A0	5
A17	A3	A2	6
A18	A5	A4	7
A19	A7	A6	8
A20	A9	A8	9
A21	A11	A10	10
A22	A13	A12	11
A23	A15	A14	12
N/D	N/D	IRQ	13
N/D	N/D	NMI	14
N/D	N/D	N/D	15
N/D	N/D	N/D	16
N/D	VB	R/W	17
N/D	N/D	HB	18
N/D	D8	D0	19
N/D	D9	D1	20
N/D	D10	D2	21
N/D	D11	D3	22
N/D	D12	D4	23
N/D	D13	D5	24
N/D	D14	D6	25
N/D	D15	D7	26
N/D	N/D	N/D	27
N/D	BE	INHRAM	28
N/D	-5v	-5v	29
N/D	+12v	+12v	30
N/D	-12v	-12v	31
GND	GND	GND	32

Bus pins used by this card are :-

a, b, & c 5 to 12
a3
a17
b17 as output if linked
a18 as output if linked
a19 to 26
a28 an output that must be obeyed
a & b 30
a, b, & c 32
a, b, & c 1

Note : N/D = not yet defined

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