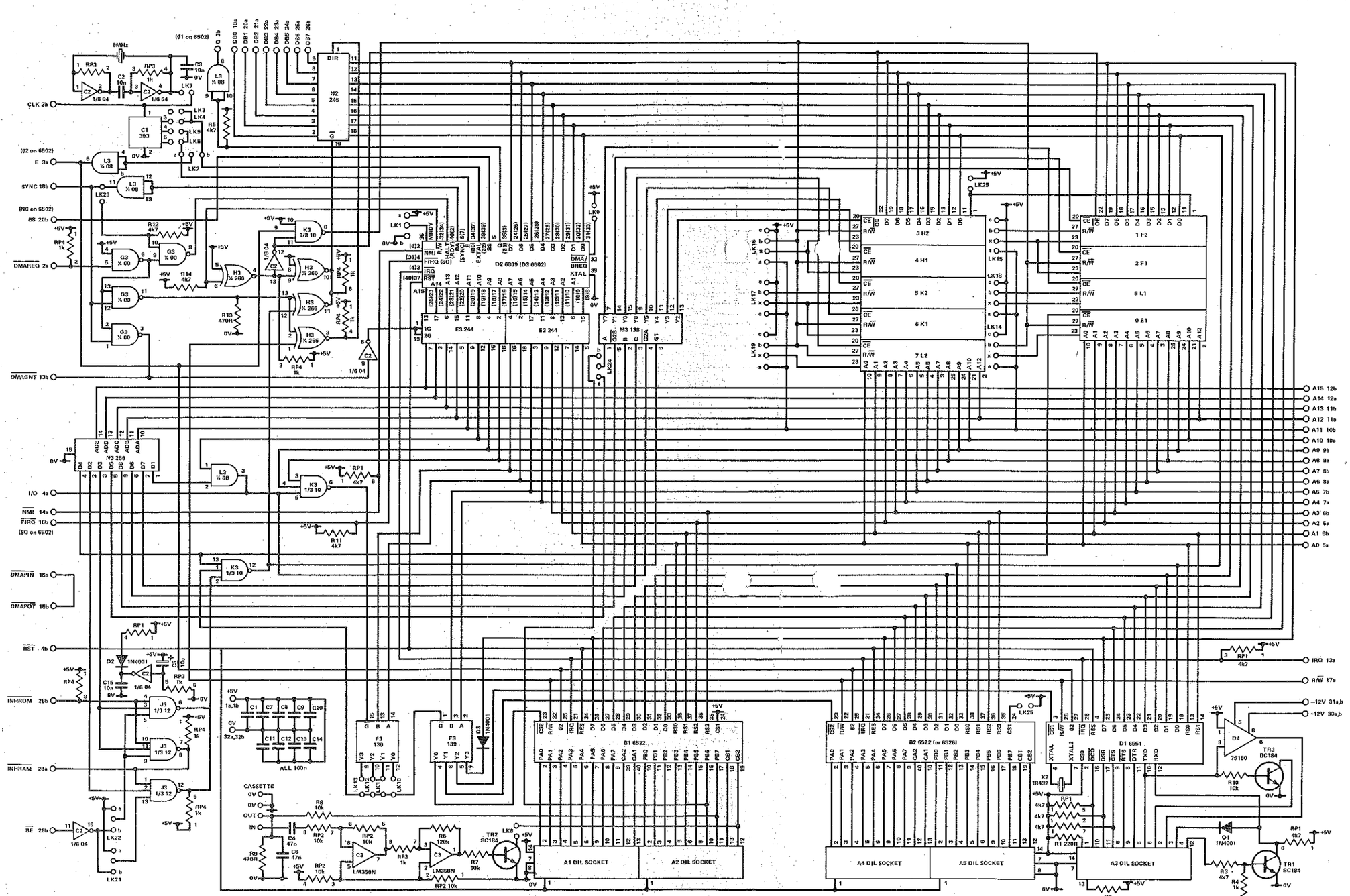
HOW IT WORKS

Fig. 1 Circuit diagram of the Single Board Controller. The numbers in brackets are the pin numbers of alternative devices, the 6502 which can be used instead of the 6809 and the 6526 instead of the 6522.



The heart of the circuit is either D2, the 6809 processor or D3, a 6502 (6802 or 6808) processor, these two using slightly offset sockets. On the circuit diagram (Fig. 1) the two possible processors are shown as one block, the pin numbers and functions for the 6502 option being shown in brackets (where different from the corresponding 6809 functions) next to the 6809 pin numbers and functions. LK1 is used for enabling or disabling on chip RAM if the 6802/6808 is in use and LK9 allows a battery supply to be used with this same processor for power down data retention. The processor clock is provided by the circuitry around C1, a binary counter and its associated crystal oscillator. LK7 selects either the on-board crystal oscillator or an off-board master clock. LK3, LK4, LK5 and LK6 select the processor frequency and LK2 alters the clock configuration depending on the type of processor in use. The power-on reset circuit is the portion including one-sixth of C2, D2 and capacitors C5 and C15. Buffering of the address bus is provided for on-board and external use by E2 and E3 whereas N2 buffers the data bus for off board peripherals only. E1, F1, F2, H1, H2, K1, K2, L1 and L2 are sockets for JEDEC memory devices, the specific type of device in use being specified by links LK14-19, some of which control a single socket and some of which affect a pair of memory sockets. The chip select decoding of these memories comes from M3, a 3 to 8 line decoder which is used in conjunction with N3, a bipolar PROM which controls the memory mapping of the complete board. LK24 allows a 2 page memory configuration to be implemented on board, the page selection being controlled from B1, a 6522 VIA. The circuitry around J3 allows on board memory to be enabled or disabled via the external BE (block enable) signal which is generated on the system mother board and allows a paged memory configuration greater than 64K to be achieved. LK21 and LK22 allow this facility to be disabled for on-board EPROM or RAM respectively. The same circuitry is sensitive to the Tanbus Inhibit RAM and Inhibit ROM signals which other boards may generate under various circumstances to disable portions of on-board memory. B1 and B2 are the 6522 VIAs, connection to the outside world being made via the DIL sockets A1, A2, A4 and A5. Socket B2 can take a 6526 in place of the 6522; this device has time of day registers and requires a 50Hz clock which may be connected via LK25. The cassette interface is driven from B1 and the circuitry round C3, an LM358N op-amp. D1 is the 6551 UART, access to which is provided via DIL socket A3 and the circuitry around D4, T33 and Tr1 provides RS232 (transmitted and received data only — not modem control lines) and 20mA current loop signal levels. The address decoding for the I/O devices is provided by F3 while links LK10-13 allow four optional addresses for the on-board portion of the I/O area. The I/O area select signal is also made available to off-board devices via the edge connector. Provision is made for DMA, the circuitry comprising G3 and H3 taking DMA request and generating DMA granted.