

MT65 High Resolution Graphics

Sheet: Video RAM



File: MT65_HRG_VRAM.sch

Sheet: Video Shifter



File: MT65_HRG_SHIFTER.sch

Sheet: Address Multiplexer

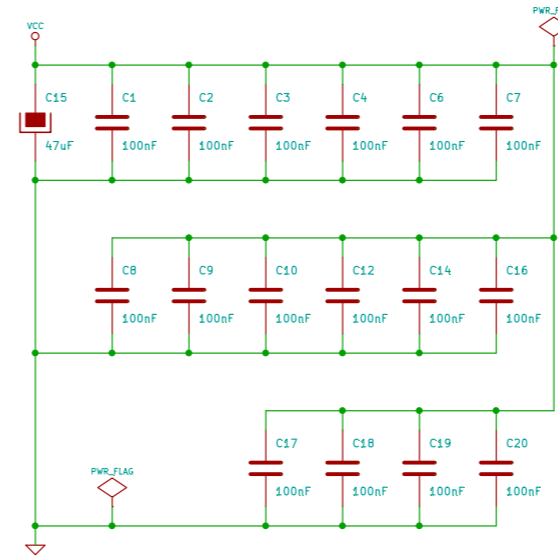


File: MT65_HRG_ADMUX.sch

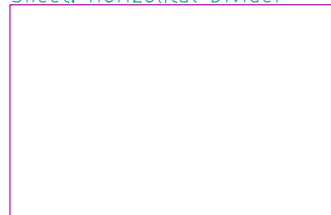
Sheet: Video Output



File: MT65_HRG_VIDEO.sch



Sheet: Horizontal Divider

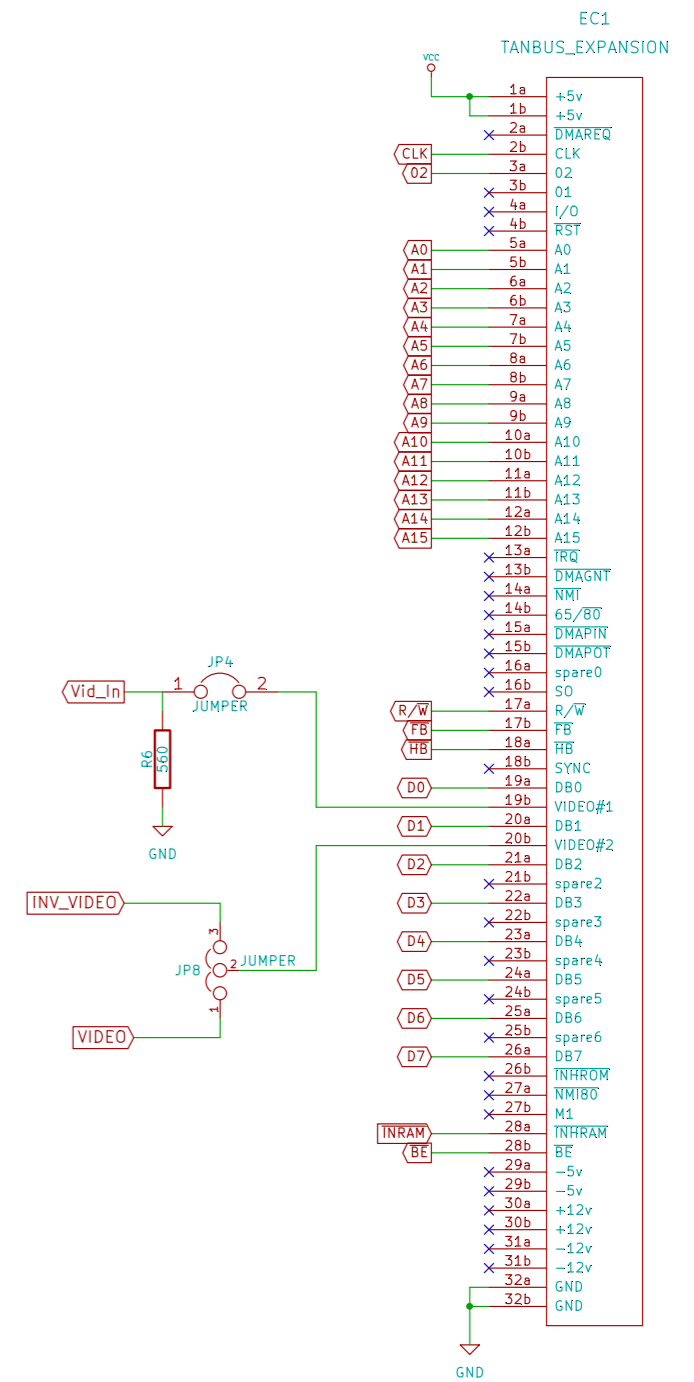


File: MT65_HRG_H-DIV.sch

Sheet: Vertical Divider



File: MT65_HRG_V-DIV.sch

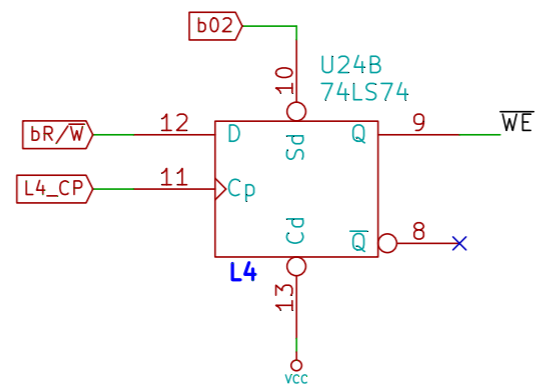
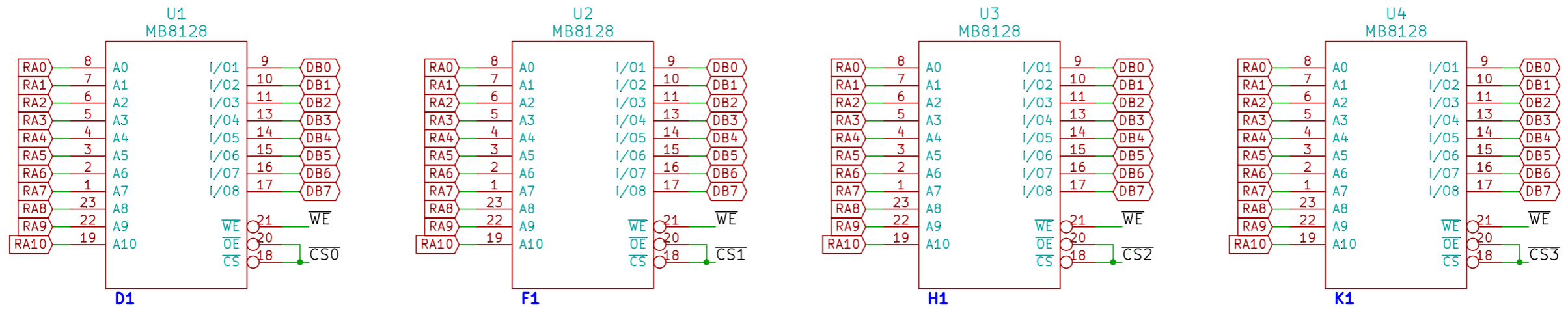


- X-O P1
- X-O P2
- X-O P3
- X-O P4

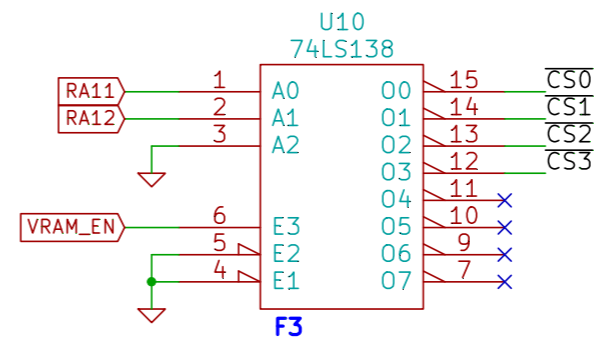
Mounting Holes

File: MT65 HRG.sch		
Sheet: /		
Title: MT65 HRG-R		
Size: A3	Date: 30 sep 2019	Rev: v1.0b
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Video RAM

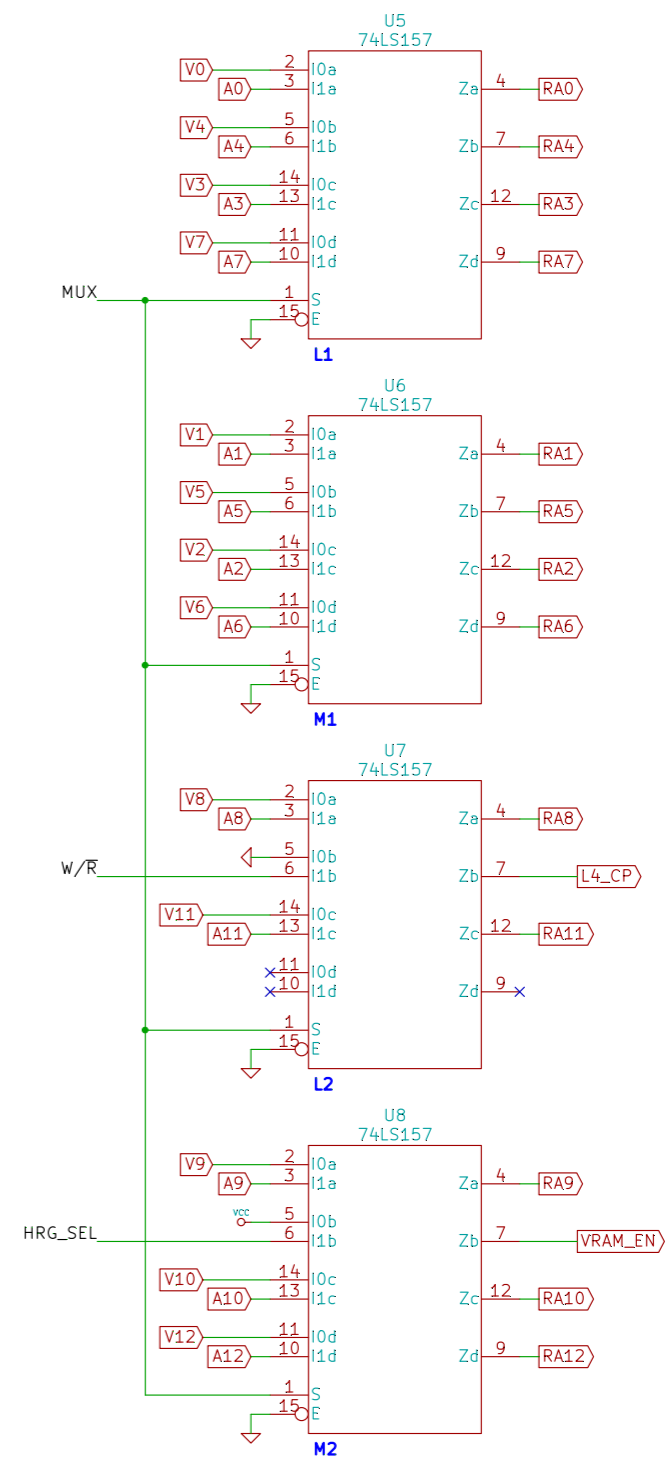
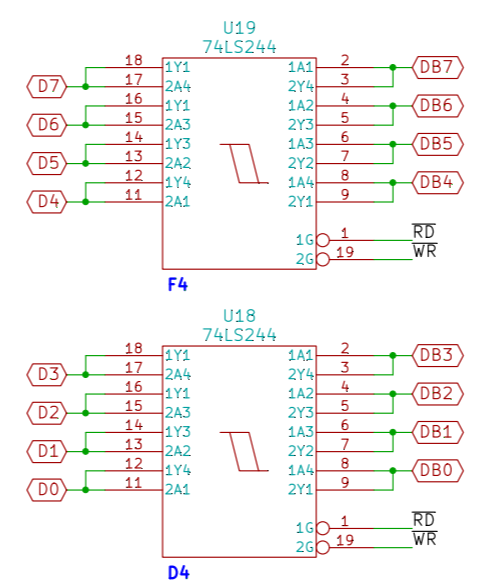
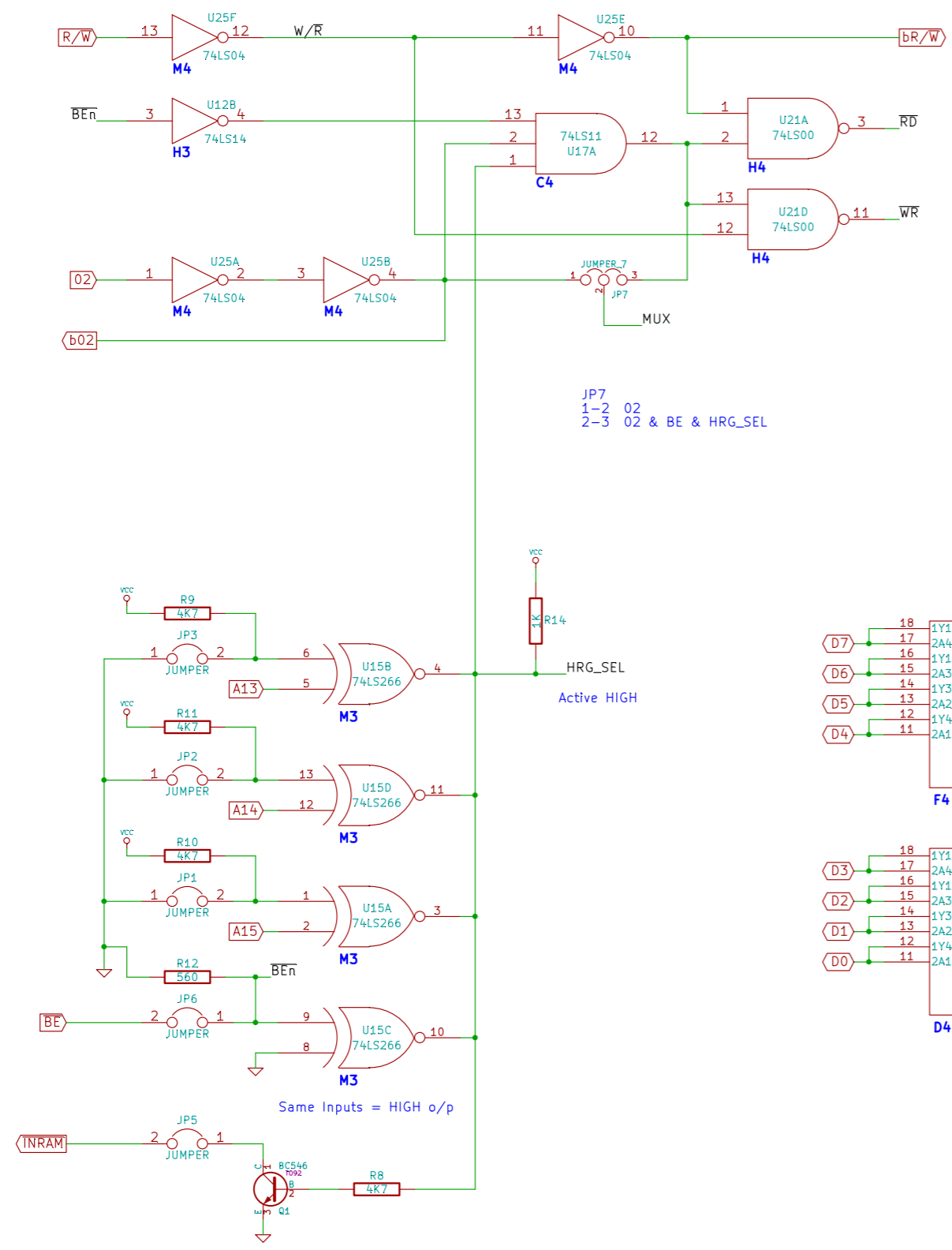


Data tx to o/p on pos CLK edge
ie pos edge of Write cycle during TANBUS addressing



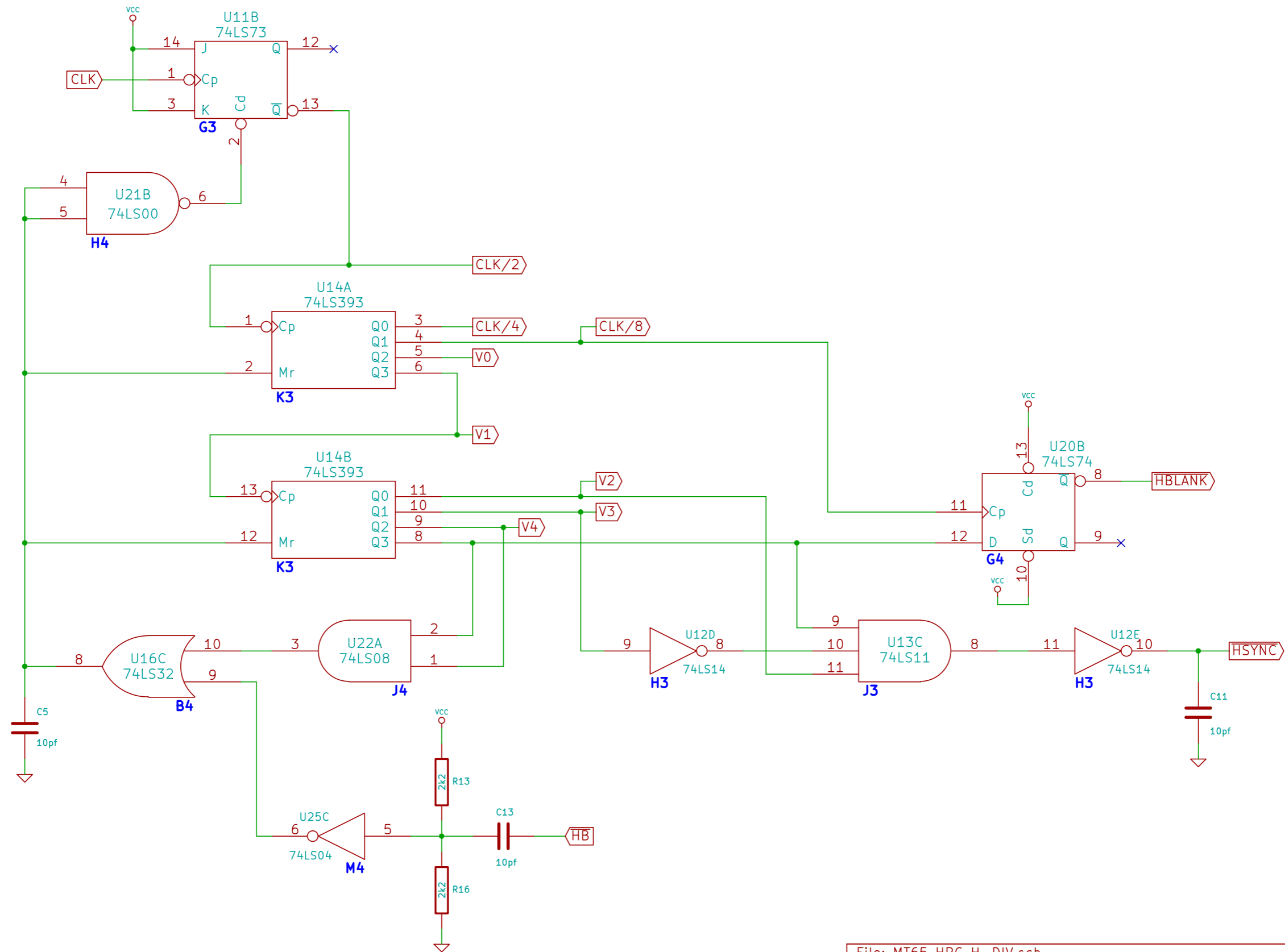
Output is LOW when RAM chip address is selected

Address MUX



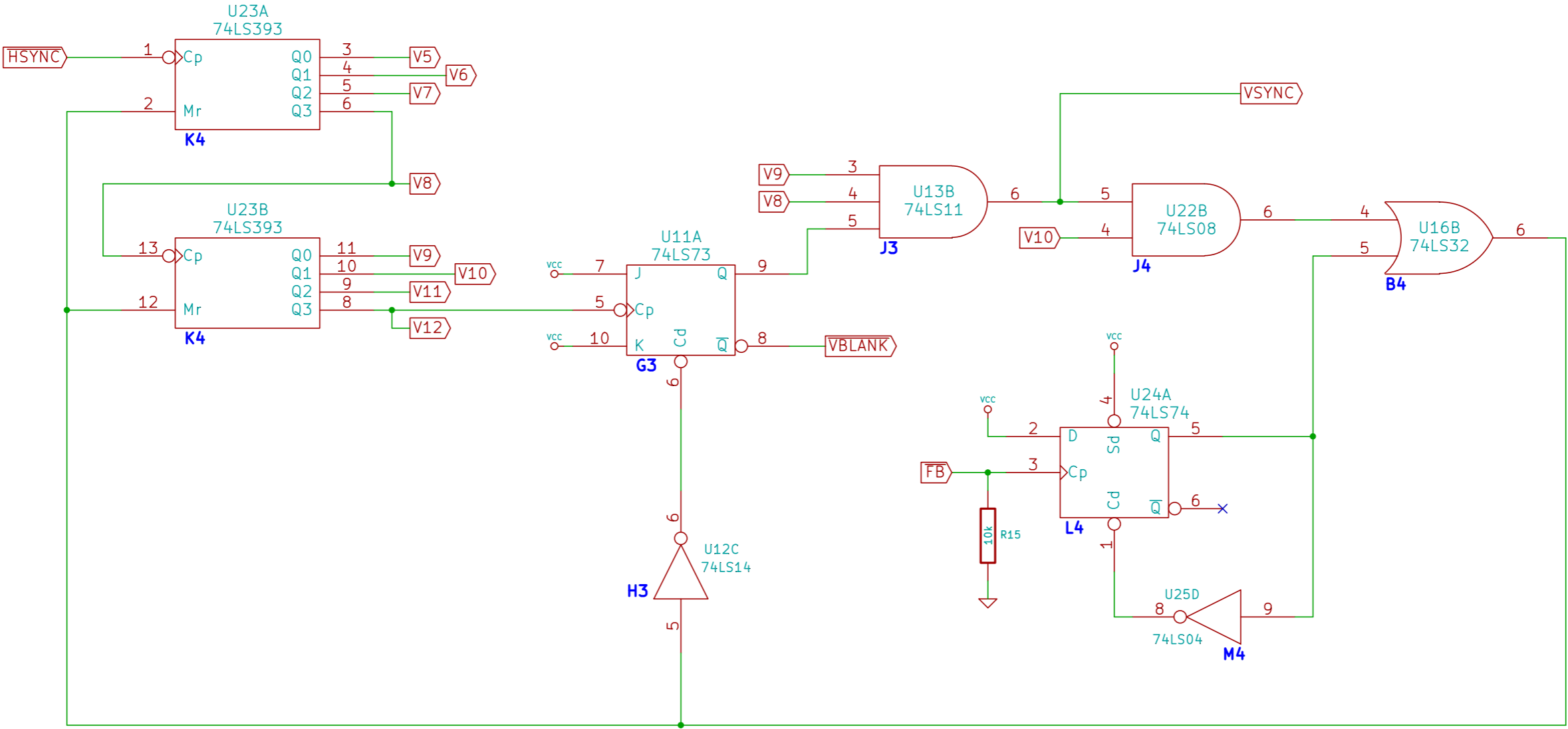
S HIGH = TANBUS Addressing (O2 HIGH)
 S LOW = VIDEO RAM addressing (O2 LOW)

Line Timebase Divider

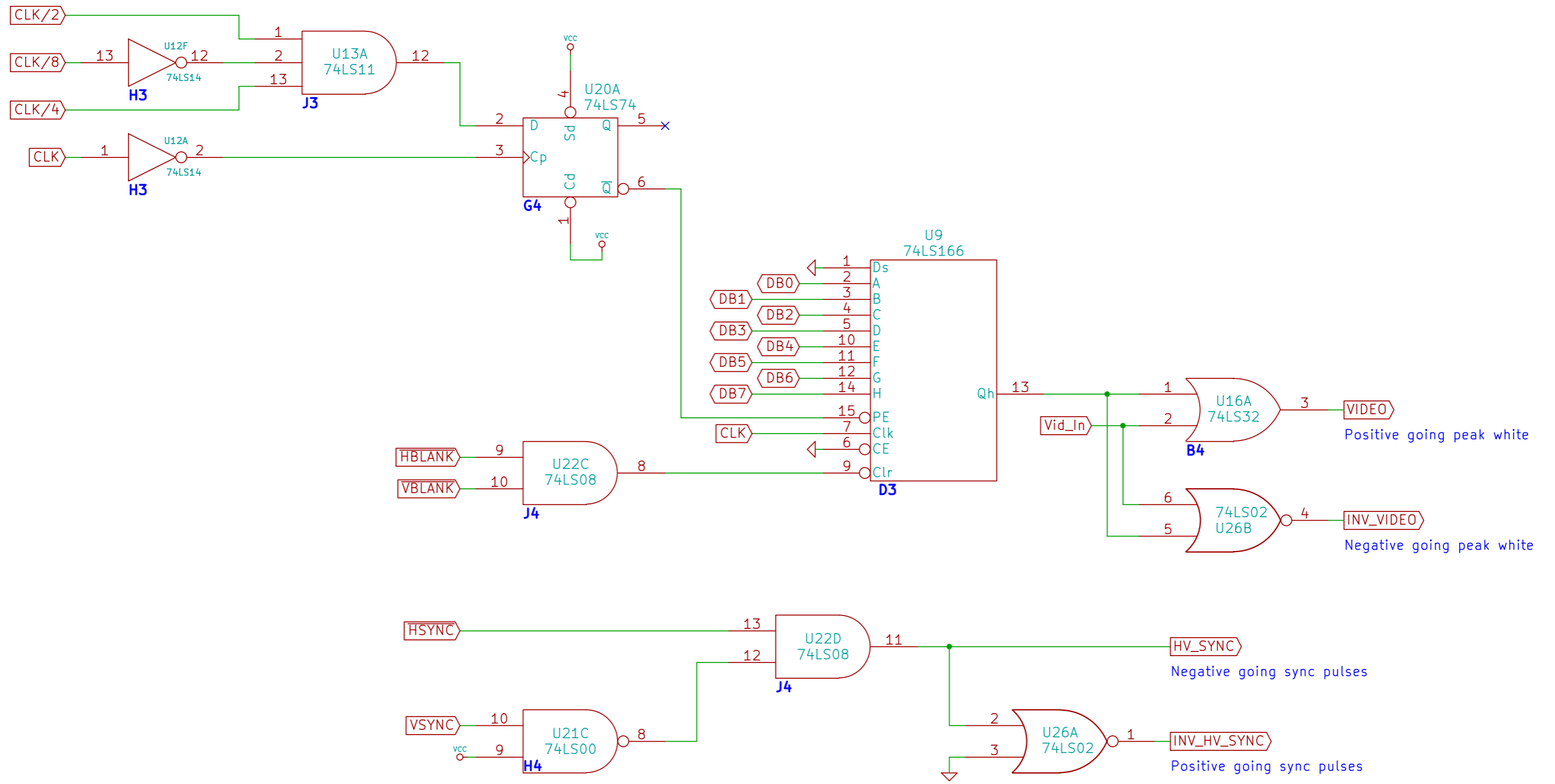


File: MT65_HRG_H-DIV.sch		
Sheet: /Horizontal Divider/		
Title:		
Size: A4	Date: 30 sep 2019	Rev:
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Frame Timebase Divider

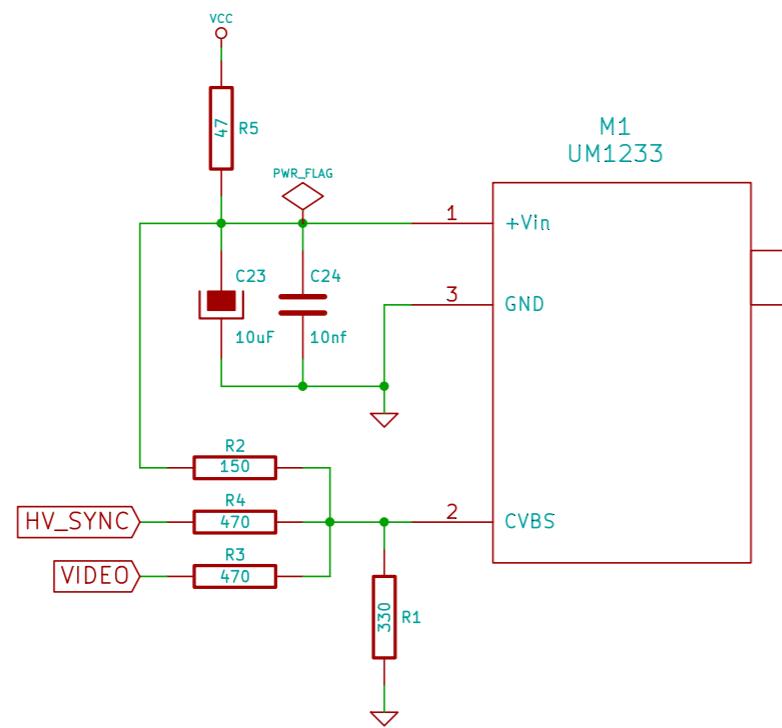


Video Data Shifter

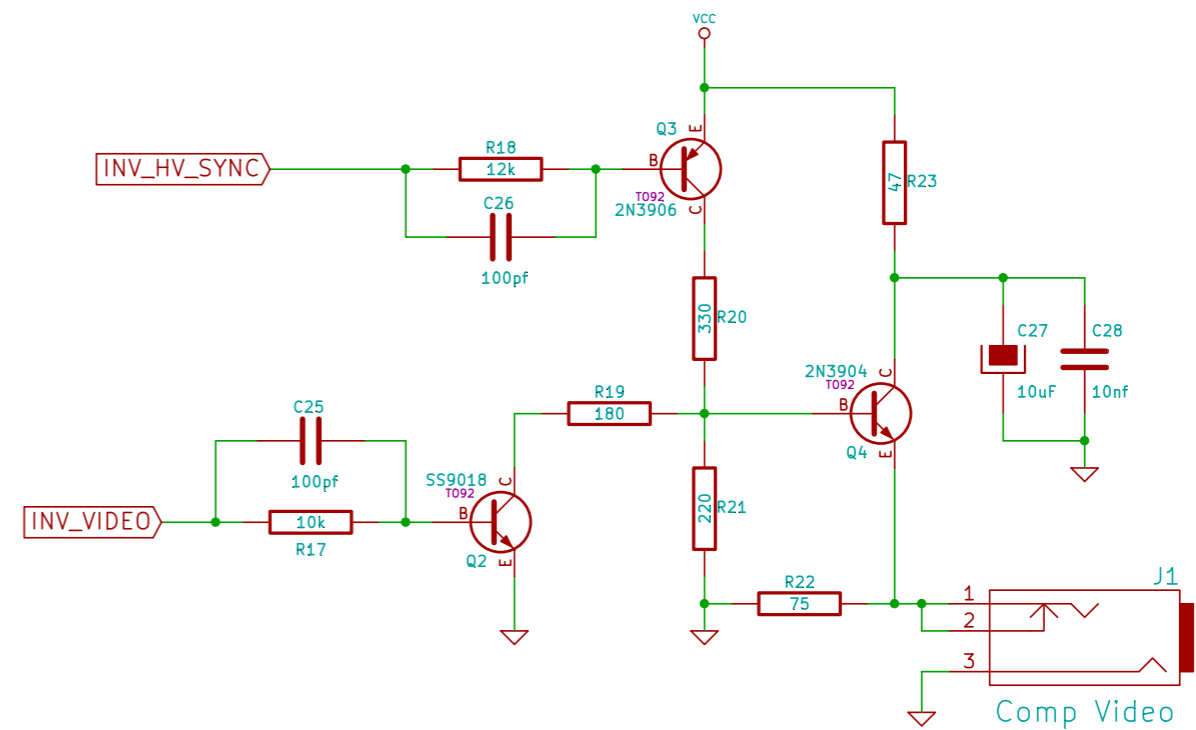


Video Output

Option [A]



Option [B]



File: MT65_HRG_VIDEO.sch

Sheet: /Video Output/

Title:

Size: A4 Date: 30 sep 2019

Rev:

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Id: 7/7