MT65 CPU Single Board Configuration and TUGBUG

When the Microtan CPU board is in single board configuration (ie no TANEX and its RAM, ROM and IO links closed), it will not operate with TUGBUG as its monitor. If tried, the board will remain held in Graphics mode, both following a Reset and a keyboard key press. The reason for this is that TUGBUG tries to access additional IO memory addresses located on other TUG boards. In single board configuration, the CPU interprets these as CPU board IO addresses because the 16 Microtan 65 IO addresses are repeated between $8000 and $BFFF - refer to page 3-3 of the Microtan 65 (CPU) manual (http://www.microtan.ukpc.net/M65-Manual.PDF).

Following a reset, the processor jumps to TUGBUG code commencing at 'START' $FC00. At location $FC22, the code jumps to the 'Send character' sub-routine at $FBEB. This subroutine immediately checks to see if the Video 80 board is present using the command BIT VDUSTA. VDUSTA is the IO memory location $BE00 on the Video 80 board. The CPU board interprets this command a 'READ' instruction at location $BFF0, ie SET Graphics mode.

Following a keyboard press, the processor jumps to the Keyboard interrupt handler 'KBINT' code commencing at $FEC2. At $FED2, the program jumps to TRYSRI sub-routine at $FB03 to check if the interrupt was caused by input via the serial port on the TANEX board. At $FB0E the program loads data from the serial port register at $BFD0. The CPU board interprets this command a 'READ' instruction at location $BFF0, ie SET Graphics mode.

With a TANEX board present and the IO link on the CPU board open, the above two miss-interpretations would not happen as the selection of CPU board IO memory is controlled by TANEX via the IOE TANBUS signal. Therefore repetitions of their IO addresses do not occur.