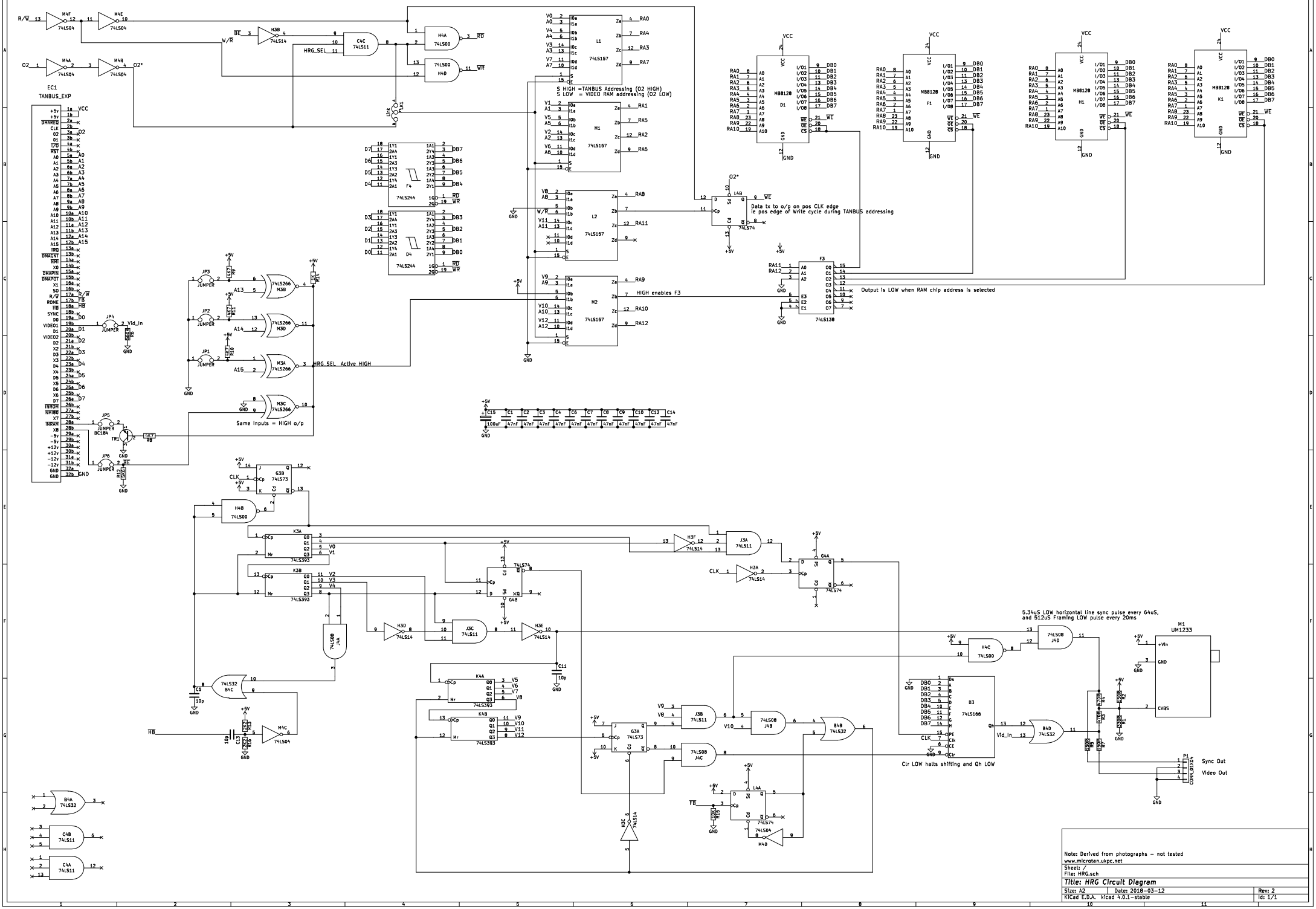
EC1
TANBUS_EXP
S HIGH =TANBUS Addressing (O2 HIGH)
S LOW = VIDEO RAM addressing (O2 LOW)
Data tx to o/p on pos CLK edge
le pos edge of Write cycle during TANBUS addressing
Output is LOW when RAM chip address is selected
HRG_SEL Active HIGH
HIGH enables F3
Same Inputs = HIGH o/p
5.34uS LOW horizontal line sync pulse every 64uS,
and 512uS Framing LOW pulse every 20ms
Clr LOW halts shifting and Qh LOW
Sync Out
Video Out
Note: Derived from photographs — not tested
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Sheet: /
File: HRG.sch
Title: HRG Circuit Diagram
Size: A2
Date: 2018-03-12
Rev: 2
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