HRG Circuit Description

Overview

The Tangerine High Resolution Graphics (HRG) board provides a 256 x 256 pixel graphics display on a domestic UHF Television or directly into a video monitor. The text and chunky graphics video generated by the Microtan 65 CPU board can be mixed with the HRG video. The HRG display picture is stored on 4 MB8128 RAM ICs.

During period when O2 is HIGH, the HRG RAM is accessible via TANBUS. When O2 is LOW, the HRG memory is sequentially addressed by a set of counters to enable the data in memory to be read and the High Resolution Graphic picture to be generated. Four 2-input multiplexers ICs L1, M1, L2 & M2 switch the RAM address lines under the control of the O2 signal between the TANBUS address lines and those generated by the counters.

TANBUS Addressing

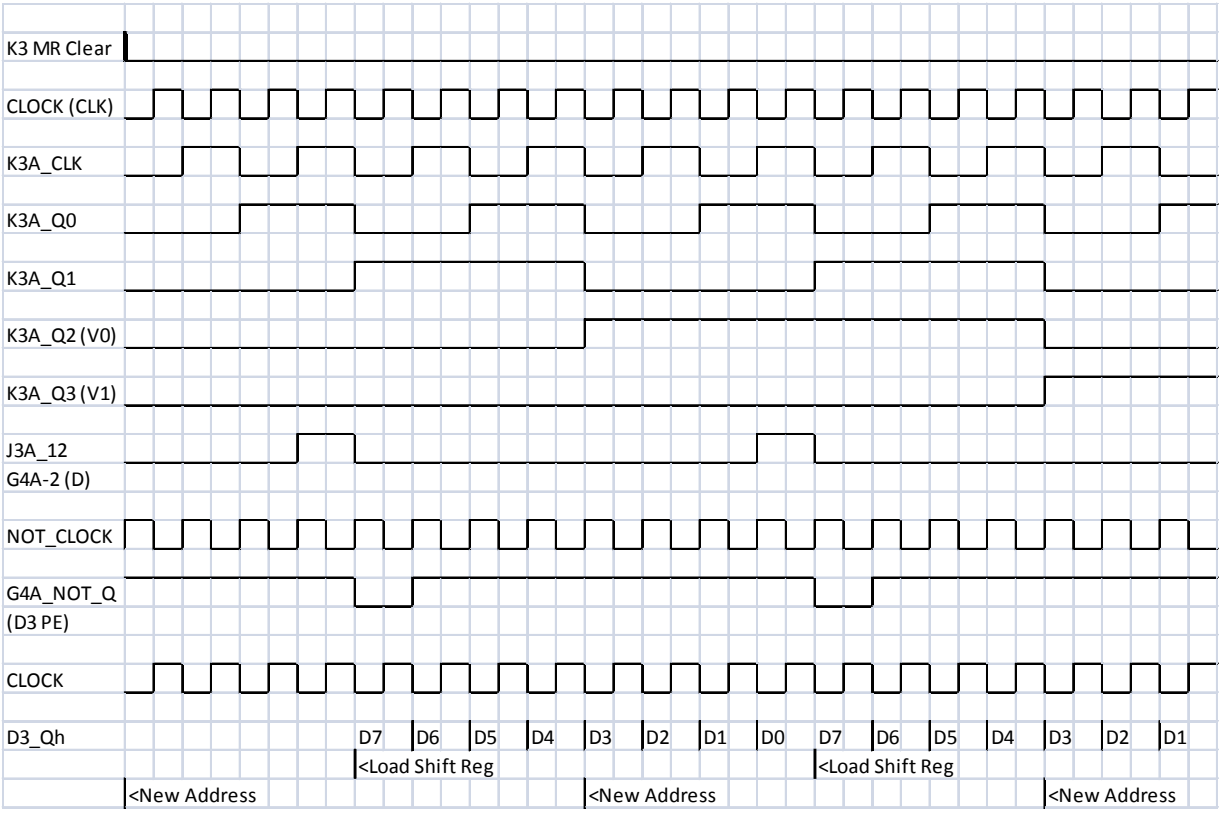
IC M3 detects when the HRG is being addressed, generating an HRG_SEL (active high) signal and provides an INHRAM signal back to the Microtan system.

IC C4c controls when the memory can be accessed by the Microtan system. BE must be LOW, HRG_SEL HIGH and O2 HIGH. ICs 4a and 4d generate the WR (write) and RD (read) signals used by the two Data Directional Buffers ICs F4 and D4 to control data directional flow to/from the TANBUS.

IC F3 is a 1-of-8 decoder and selects which of the 4 memory ICs is being addressed as determined by the RAM address lines RA11 and RA12. F3 is always enabled when O2 is LOW, but only if HRG_SEL is HIGH when O2 is HIGH (TANBUS addressing).

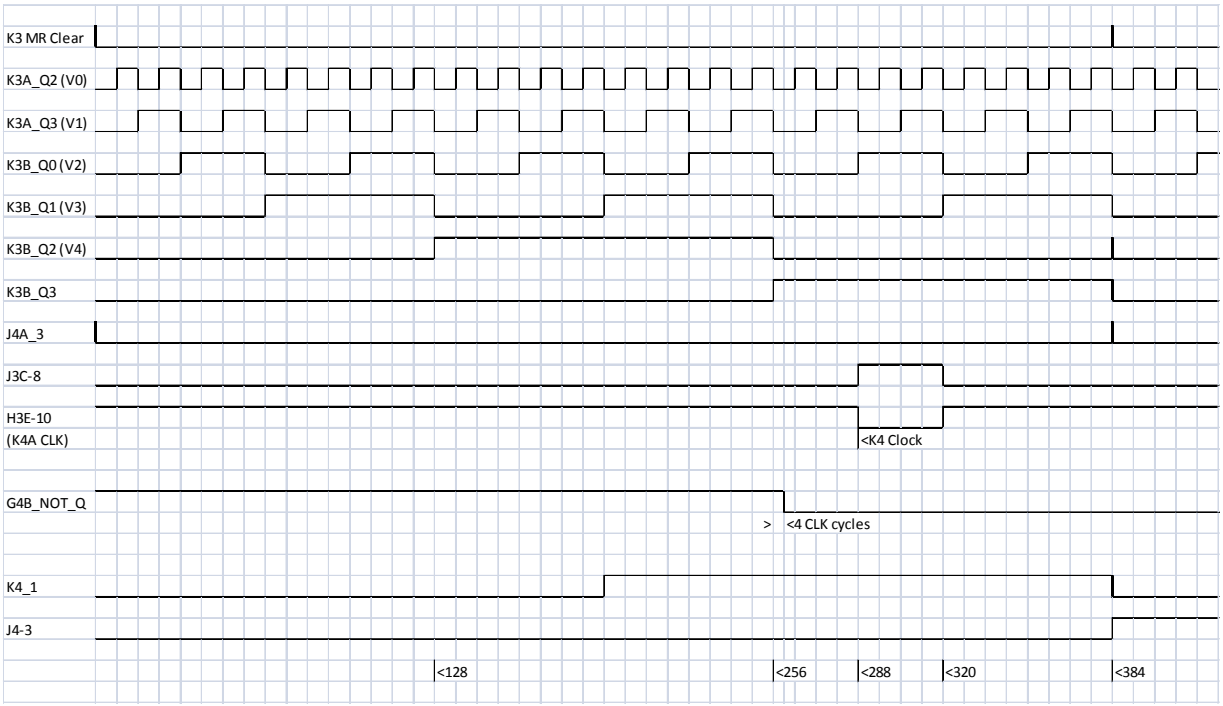
The 4 RAM ICs have a WE signal which controls whether the memory is being read (WE HIGH) or written to (WE LOW). This is generated at the Q output of the D-type (positive edge) Flip-Flop IC L4b. The Flip-Flop (and WE) is Preset HIGH when O2 goes LOW allowing the memory to be read to generate the High Resolution picture. Its D input follows the TANBUS R/W signal. It is only clocked when O2 is HIGH (TANBUS addressing) and W/R goes from LOW to HIGH (start of the Write cycle). At this time, R/W (the D input) has just gone LOW and so the Flip-Flop Q output (WE) goes LOW. This remains until O2 goes LOW and the Flip-Flop Presets HIGH again.

High Resolution Picture Generation



The counters used to sequentially address the HRG RAM to generate the High Resolution picture are driven by the 6MHz TANBUS Clock (CLK) signal. This is first divided by 2 by the J-K Flip-Flop IC G3b. The Binary counter IC K3 divides this signal by 4 and then generates the first 5 low-order RAM addresses (V0 - V4) which represents one horizontal line of data (32 memory locations x 8 bits) of the high resolution picture. V0 is CLK divided by 8 and the full line of data is addressed every 256 CLK cycles.

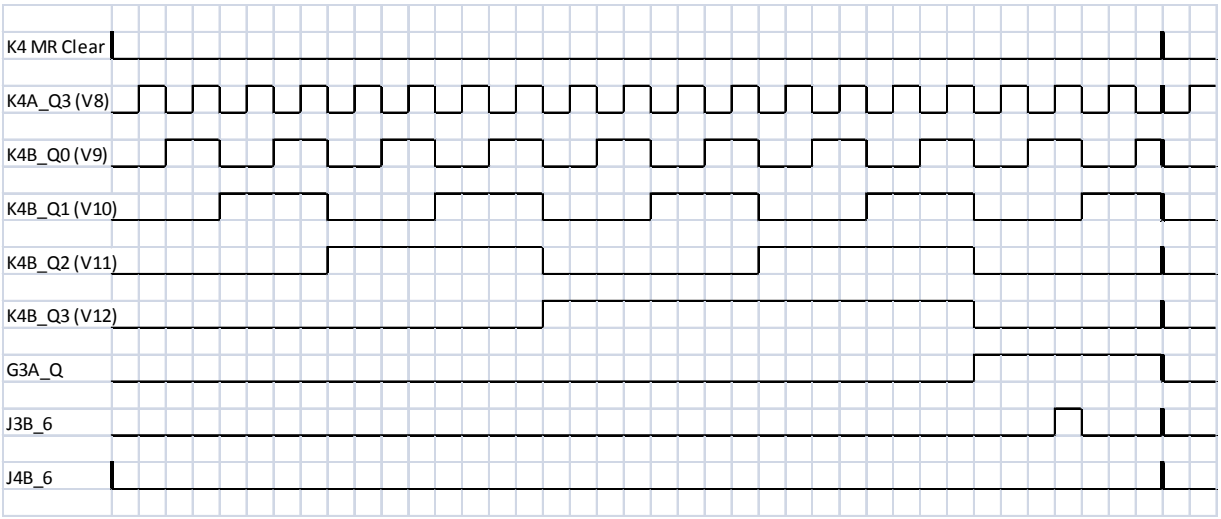
The AND gate IC J3a generates a HIGH pulse 3 CLK cycles after the V0 address line changes. This is fed into the D-type Flip-Flop IC G4a which generates a LOW pulse one CLK cycle later (ie 4 CLK cycles after the V0 address line changes). The parallel data inputs (DB0-DB7) are loaded in the Shift Register IC D3 on the negative edge of this pulse. DB7 is immediately presented on the Shift Register output and the other data is shifted out sequentially on the positive edge of the CLK signal. A new set of data is loaded into the Shift Register every 8 CLK cycles.



IC K3 further divides V4 by 2 (output Q3), which is AND gated with V4 by IC J4a to generate the counter reset signal after 384 CLK cycles (equivalent to 64uS and 15.625KHz PAL Horizontal scanning rate). OR Gate IC B4c uses either this reset signal or the external Horizontal Blanking (HB) signal inverted by IC M4c to reset the G3b Flip-Flop and the K3 counters. This enables the HRG High Resolution Picture lines to be synchronised with video generated by the Microtan CPU board.

ICs J3c and H3e generate a LOW pulse between 288 and 320 CLK cycles. This is used as the horizontal line video sync pulse. Also, the negative edge of this pulse clocks the next set of binary counters (IC K4) which generate the upper-order RAM addresses (V5 - V12).

Figure 1 shows that IC K3a-Q1 goes HIGH after completion of the first 4 CLK cycles. This is used as the Clock input for the D-Type Flip-Flop IC G4B which uses the IC K3B-Q3 output as its D input. This in turn generates a HIGH signal at its non-inverting output 4 CLK cycles after the counters are reset ie to coincide with data being shifted out of the shift registers. This remains HIGH until the full line of data has been addressed (ie when IC K3B-Q3 has gone LOW) and the next positive clock pulse is received (ie a further 4 CLK cycles have passed). This remains LOW until 4 CLK cycles after the counters are reset again. This provides an HRG Horizontal Blanking Signal.



JK Flip-Flop G3a goes HIGH on its non-inverting output immediately after all the RAM memory has been addressed.

This is AND gated with V8 and V9 by J3b to generate a positive pulse of 512uS duration, 1.536mS after all the RAM memory has been addressed.

JK Flip-Flop G3a non-inverting output is also AND gated with V8, V9 and V10 by J3b and J4 to generate a positive pulse reset signal. OR Gate IC B4b uses either this reset signal or one generated by D-type Flip-Flop L4a from the external Frame Blanking (FB) signal to reset the G3a Flip-Flop and the K4 counters. This enables the HRG High Resolution Picture frames to be synchronised with video generated by the Microtan CPU board.

JK Flip-Flop G3a goes LOW on its inverting output immediately after all the RAM memory has been addressed.