TANBUS Signal Descriptions

6502 Microprocessor signal lines

A0-A15	Address bus. Normally driven by the CPU board but handed over to a peripheral device when it performs a direct memory access.
D0-D7	Microtan 65 system data bus which connects only to TANEX. Not buffered.
DB0-DB7	System data bus buffered from the CPU board on the TANEX.
CLK	6MHz clock out put from CPU board. Not buffered.
ϕ_1	Microprocessor clock phase 1 output from CPU board. Not buffered.
ϕ_2	Microprocessor clock phase 2 output from CPU board. Not buffered.
SYNC	The 6502 microprocessor sync signal which goes high during ϕ_1 of an OP CODE instruction fetch and stays high for the remainder of that cycle. Not buffered.
	Note: above 4 signals are buffered on the Tangerine MT010 motherboard.
R/W	Read not Write. Driven by the CPU board to indicate whether the 6502 microprocessor is reading or writing to the data bus. Handed over to a peripheral device when DMAs are performed.
RST	Normally HIGH, active LOW. Used to reset the complete Microtan system including the microprocessor. When TANRAM or any peripheral device with dynamic memories is being used the reset line must only be active for about 10uS.
IRQ	Interrupt request. An open-collector line used by devices requesting a CPU microprocessor interrupt.
NMI	Non-maskable interrupt. Used and driven by the delayed non-maskable interrupt circuitry on the CPU board. If the user wishes to use non-maskable interrupts in specialist applications, then link LKNMI on the CPU board should be broken and this line driven by a peripheral device with an open collector.
RDY	Ready. This input signal allows the user to halt the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with Phase ϕ_1 will halt the processor with the address lines reflecting the current address being fetched. This condition remains through subsequent Phase ϕ_2. If RDY is low during a write cycle, it is ignored until the following read operation. RDY transitions must not be permitted during ϕ_2 time. On the TANBUS, RDY signal on the CPU board is connected to the DMAREQ signal line on the TANEX and Expansion slots.
SO	Set Overflow Flag. A negative going edge on this signal line input to the microprocessor sets the overflow bit in the microprocessors Status Code Register. This is sampled on the trailing edge of Phase ϕ_1.

System memory management control signals

I/O — An output from TANEX to indicate that the address bus is addressing an I/O device in the range $BC00 - $BFFF. Active HIGH.

IOE — TANEX output. Active low. Indicates that the address bus is addressing RAM on the CPU board locations $BFF0-$BFFF.

RAME — TANEX output. Indicates that the address bus is addressing RAM on the CPU board locations $0-$3FF.

ROME — TANEX output. Indicates that the address bus is addressing ROM on the CPU board locations $F000-$FFFF., or if the LK1 link on the TANEX has been cut, locations $F800-$FFF. ROM only exist on the CPU board from $FC00-$FFF (Monitor EPROM).

INHRAM — Inhibit RAM. Active LOW. This signal allows, with the relevant decoding, any section of RAM to be inhibited.

BE — Block enable. This signal is generated by the MT010 motherboard memory page logic and is used as a memory page control line. An individual board can be selected from multiple circuit boards (with overlapping address ranges) fitted to the motherboard. Active LOW. Full description is available here.

Microtan display screen controls

FB — Field blanking of the television display. Driven from CPU board. For future use.

HB — Horizontal Blanking of the television display. Driven by the CPU board. For future use.

Direct Access Memory control signals

ABE — Address Bus Enable. This is the TANBUS Address Enable control signal. It is an output from TANEX to the MT65 CPU board. It is used to disable the address buffers on the CPU card so that DMAs can be performed on any memory resident on other boards in the Microtan system. It also disables the CPU board R/W buffer.

DMAGNT — An output from TANEX to indicate that the CPU has halted and the Microtan address buffers have been disabled so that the requesting peripheral may proceed with direct memory access.

DMAREQ — Direct Memory Access Request. Normally high. Used by peripheral devices to request control of TANBUS for direct memory access. When pulled LOW it halts the 6502 (via the RDY signal line) on the CPU board and flips a D Type Flip/Flop on the TANEX which in turn disables the Address & R/W buffers on the CPU board and pulls the DMAMGT signal line down LOW indicating that DMA can now take place. Before any board makes a DMA request, it should check that its DMAPIN is HIGH (ie no other higher-priority board is already making a request). If OK it should set its DMAPOT LOW at the same time as making the request.

DMAPIN Direct Memory Access priority input. Connected to the DMAPOT of the next higher-priority board.

DMAPOT Direct Memory Access priority output. Connected to the DMAPIN of the next lower-priority board. A board requesting DMA takes the DMAPOT LOW which is read at the DMAPIN of the next lower priority board to indicate that it must wait for it to return HIGH before making its own DMA request. While waiting, it in turn makes its DMAPOT LOW to pass on down the chain.

DMAPIN and DMAPOT connections on peripheral boards form a daisy chain which are used to determine the priority of peripherals requesting DMA. The board nearest the MT65 CPU receives the highest priority. Boards not using these signals should connect the two pins together.

Legacy DOS signals used when the legacy disc controller board was fitted in the DOS slot in the early Tangerine motherboards. Note: they are not used by the later TANDOS board that is fitted in any of the expansion slots of the motherboard.

DP Disc present. This is a system control line that indicates that the legacy disc controller card is present in the system.

65/80 The legacy disc controller board incorporated a Z80 microprocessor. This line defines which processor is active.

NMI80 This is a Z80 control signal for non-maskable interrupt and is independent from the 6502 non-maskable interrupt.

MI This is a Z80 control signal that indicates the start of a new machine cycle and is equivalent to the 6501 SYNC signal.