TANRAM

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INTRODUCTION

Tanram is a 40K RAM Card designed to upgrade the Microtan, Tanex combination to a 48K system. The fully expanded board contains two 16K blocks of dynamic RAM and a 7K block of Static RAM. Tanram has on board memory refresh logic and therefore will not slow down the processor. To the processor Tanram appears as a Static RAM Card.

The cards' memory map is designed to appear at the end of the Tanex memory (2ØØØH) and occupies the area of unused address space up to the beginning of the I/O ports (BBFFH).

Tanram is available in a minimum configuration with one 16K block of dynamic RAM (2ØØØH - 5FFFH) or fully expanded as a 40K Card.

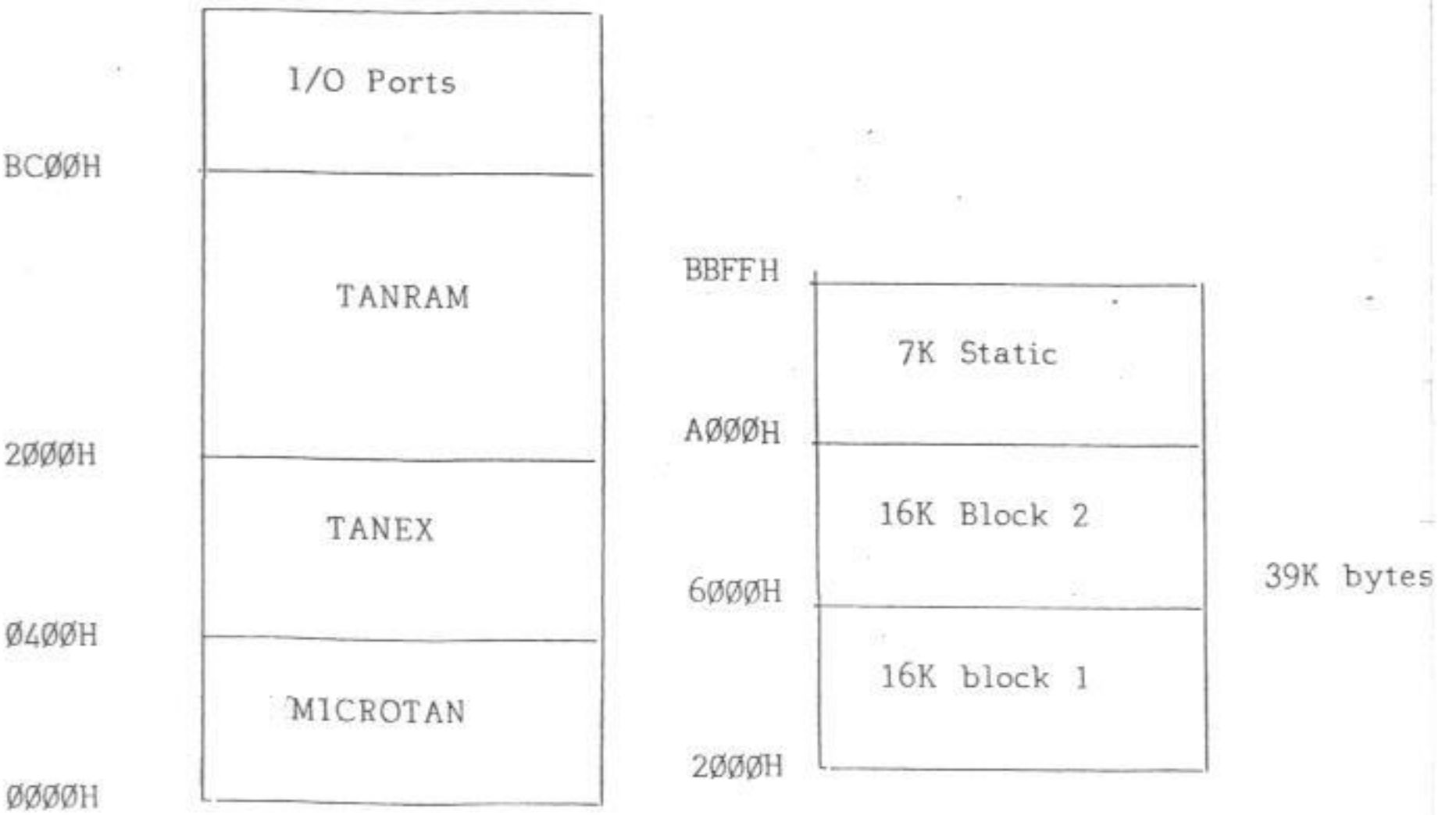


Figure 1 Tanram Memory Map

2) FEATURES AND SPECIFICATION

a) Tanbus Compatible.

b) Upto 40K of RAM organized as two blocks of 16K dynamic, and one block of 7K Static; all devices industry standard 2114's and 4116's.

c) Available in a minimum configuration of 16K (contiguous with Tanex memory) or fully expanded to 40K.

d) Transparent refresh; does not slow processor down.

e) Operates at 750KHz or 1MHz bus speeds.

f) Low power consumption:

16K Version -	+5V	@	330mA
	+12V	@	20mA
	-5V	@	<1mA
40K Version -	+5V	@	1.0A
	+12V	@	30mA
	-5V	@	<1mA

g) Memory map contiguous with Microtan 65, Tanex combination.

h) Block enable input (BE) allows individual pages of memory to be selected from motherboard.

i) Inhibit RAM input (INHRAM) allows memory to be disabled so that ROM may exist within Tanram memory map.

3) HARDWARE DESCRIPTION

Dynamic Ram Section

Memory Cycle:

The 6502 sets valid DATA, ADDRESS, and $\overline{R/W}$ halfway through Ø2 (low). This allows the decode section approx. 500ns set up time, when Ø2 goes high this starts the appropriate memory cycle, and enables the Data Bus Buffers.

A monostable, 74123, is used to generate the two $\overline{RAS}$ signals, 1st for memory cycle, 2nd for refresh cycle. The Address decode logic provides the Block enables which qualifies memory access $\overline{RAS}$, to the selected Block. A chain of four schmitt inverting gates with R.C. Delays provide two $\overline{RAS}$ signals each delayed by 40ns. The first is used to switch the multiplexer. The second is used to generate $\overline{CAS}$ via an R-S flip flop, which is reset by the falling edge of memory cycle request.

Refresh Cycle

4116 Dynamic memories need refreshing every 2ms (min.). We have chosen the 128 cycle $\overline{RAS}$ only refresh method.

The Refresh request signal is derived from Ø2 divided by 10, which gives us a 1.7ms refresh period. The refresh request is only active when Ø2 is low, which makes it completely transparent as far as the 6502 is concerned. When the refresh cycle request is active the multiplexer internally switches to the refresh counter. The $\overline{RAS}$ is generated by the second half of the monostable, 74123, this takes approx. 400ns, after which the request is removed allowing 200ns set up time for the next memory access. Refresh $\overline{RAS}$ is forced on both blocks irrespective of Block select.

Static RAM Section

The Static RAM section of TANRAM acts in the same way as the 7K block on Tanex, requiring no special signals. The static area on TANRAM can be added to in 1K increment (see figure 4).

Memory Speed

Tanram is capable of being operated at ¾MHz or 1MHz; in either case the static memory can be of the lower cost 450ns variety.

When operating at ¾MHz the dynamic memory devices can be 300ns version. However at 1MHz bus speeds the 250ns variety must be used.

All dynamic memory devices supplied by Tangerine will be the 250ns version, irrespective of operating speed.

4) THE BUS INTERFACE

Tanram was designed to interface to TANBUS, the Standardised Tangerine expansion bus (see figure 3).

The only processor signals Tanram requires are the two clocks Ø1 and Ø2.

Three other signals, $\overline{\text{INHRAM}}$, $\overline{\text{BE}}$ and I/O are required to enable the card; a truth table for these signals is given in figure 2.

$\overline{\text{INHRAM}}$ (Inhibit RAM) This signal is taken low when another expansion card, such as the 32K ROM Card or the High Resolution Graphics Card sits in Tanrams memory map.

$\overline{\text{BE}}$ (BLOCK ENABLE) This signal is generated by the system motherboard page select logic. It is used as a memory page control line. An individual memory card can be selected from multiple pages of memory on the System Motherboard; It must be held low to enable card.

I/O (Input/Output) an output from Tanex to indicate that the address bus is addressing an I/O device, i.e. the address from BCØØH to BFFFH.

	SIGNAL LINE		
TANRAM MODE	$\overline{\text{INHRAM}}$	$\overline{\text{BE}}$	I/O
ENABLE	1	0	0
DISABLED	0	-	-
DISABLED	-	1	-
DISABLED	-	-	1

Key: 1 = logic 1
0 = logic Ø
- = don't care

Figure 2 Tanram enable signals

ADDITIONAL b	ADDITIONAL a		TANEX b	TANEX a		microtan 65 b	microtan 65 a
+5	+5	1	+5	+5	1	+5	+5
CLK	$\overline{\text{DMAREQ}}$	2			2	CLK	$\overline{\text{DMAREQ}}$
Ø1	Ø2	3			3	Ø1	Ø2
$\overline{\text{RST}}$	I/O	4		$\overline{\text{DMAREQ}}$	4	$\overline{\text{RST}}$	DP
A1	AØ	5	Ø1	Ø2	5	A1	AØ
A3	A2	6	$\overline{\text{RST}}$	I/O	6	A3	A2
A5	A4	7	A1	AØ	7	A5	A4
A7	A6	8	A3	A2	8	A7	A6
A9	A8	9	A5	A4	9	A9	A8
A11	A1Ø	1Ø	A7	A6	1Ø	A11	A1Ø
A13	A12	11	A9	A8	11	A13	A12
A15	A14	12	A11	A1Ø	12	A15	A14
$\overline{\text{DMAGNT}}$	$\overline{\text{IRQ}}$	13	A13	A12	13	SO	$\overline{\text{ABE}}$
65/$\overline{8Ø}$	$\overline{\text{NMI}}$	14	A15	A14	14	$\overline{\text{FB}}$	$\overline{\text{IRQ}}$
$\overline{\text{DMAPOT}}$	$\overline{\text{DMAPIN}}$	15	$\overline{\text{DMAGNT}}$	$\overline{\text{ABE}}$	15	$\overline{\text{NMI8Ø}}$	$\overline{\text{NMI}}$
SO		16	SO	$\overline{\text{IRQ}}$	16	$\overline{\text{IOE}}$	$\overline{\text{RAME}}$
$\overline{\text{FB}}$	R/$\overline{\text{W}}$	17	$\overline{\text{FB}}$	$\overline{\text{NMI}}$	17	ROME	R/$\overline{\text{W}}$
SYNC	$\overline{\text{HB}}$	18	$\overline{\text{IOE}}$	$\overline{\text{RAME}}$	18	SYNC	$\overline{\text{HB}}$
VIDEØ	DBØ	19	ROME	R/$\overline{\text{W}}$	19	DØ	VIDEØ
	DB1	2Ø	SYNC	HB	2Ø	D1	
	DB2	21	DBØ	DØ	21	D2	
	DB3	22	DB1	D1	22	D3	
	DB4	23	DB2	D2	23	D4	
	DB5	24	DB3	D3	24	D5	
	DB6	25	DB4	D4	25	D6	
$\overline{\text{INHROM}}$	DB7	26	DB5	D5	26	D7	
M1	$\overline{\text{NMI8Ø}}$	27	DB6	D6	27	$\overline{\text{INHRAM}}$	$\overline{\text{INHRAM}}$
$\overline{\text{BE}}$	$\overline{\text{INHRAM}}$	28	DB7	D7	28	M1	65/$\overline{8Ø}$
-5	-5	29	$\overline{\text{INHRAM}}$	$\overline{\text{INHRAM}}$	29		
+12	+12	3Ø	+12	+12	3Ø	+12	+12
-12	-12	31	-12	-12	31	-12	-12
GND	GND	32	GND	GND	32	GND	GND

Figure 3 Tanbus Connections

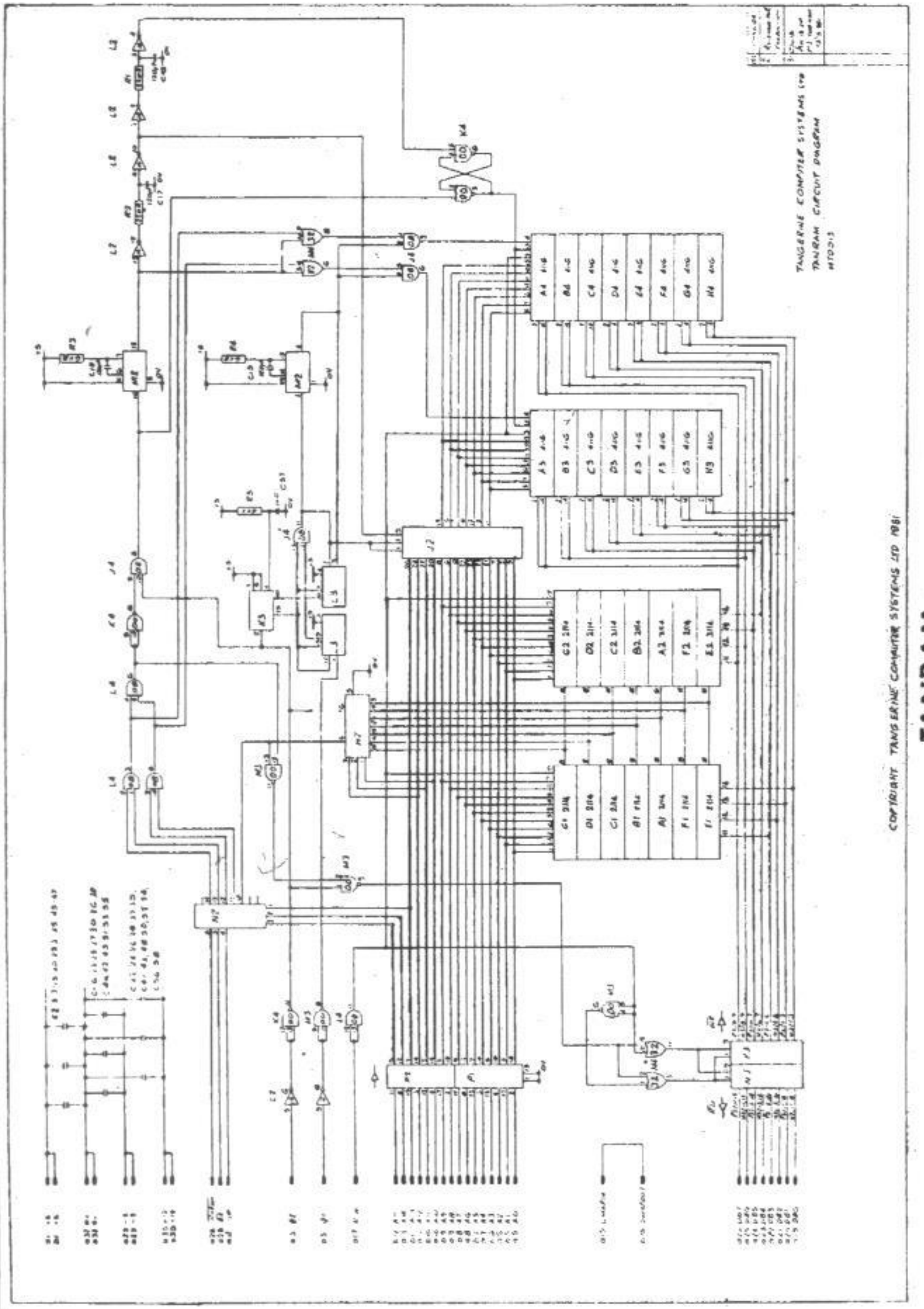
Static RAM Address Map

ADDRESS	DEVICE	I.C. LOCATION Vs. DATA BIT	
		BO - B3	B4 - B7
B8ØØ - BBFF	2114	E1	E2
B4ØØ - B7FF	2114	F1	F2
BØØØ - B3FF	2114	A1	A2
ACØØ - AFFF	2114	B1	B2
A8ØØ - ABFF	2114	C1	C2
A4ØØ - A7FF	2114	D1	D2
AØØØ - A3FF	2114	G1	G2

Dynamic RAM Address Map

ADDRESS	DEVICE	I.C. LOCATION Vs. DATA BIT							
		BO	B1	B2	B3	B4	B5	B6	B7
6ØØØ - 9FFF	4116	H3	G3	F3	E3	D3	C3	B3	A3
2ØØØ - 5FFF	4116	H4	G4	F4	E4	D4	C4	B4	A4

Figure 4 I.C. location and bit pattern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MTD313
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