PROJECT

SINGLE BOARD CONTROLLER

Mike Bedford considers the new Single Board Controller from Microtan Computer Systems Ltd and describes some simple modifications which will allow it to be used as a low-cost control computer.

Despite the increasingly large number of home computers on the market there are still surprisingly few which are aimed at the electronics enthusiast. Most machines are entirely suitable for game playing and BASIC programming, having such facilities as medium resolution colour graphics and sound effects, but they do not lend themsleves to learning about the hardware or machine code programming. One product which has become known as a "hardware man's machine" is the Microtan 65, a number of add-ons for which have been featured in ETI. One drawback of the Microtan 65 is that the design is now somewhat dated, the single board having very little memory and being based upon the 6502 processor.

Out of the same stable has now ɔme the Single Board Controller, ɥhich is being marketed by Microtanic Computer Systems Ltd. This board uses the same bus specification as the Microtan 65 and can therefore be interfaced with previous Tangerine peripheral boards, but it can also be configured to use the 6809, regarded by many as the most powerful 8 bit processor. Other suitable processors are the 6802 and the 6808 which are versions of the 6800 with on-chip clock and RAM, but in this article the discussion will be restricted to the 6502 and 6809. The controller can also take up to 56K of memory on the one board.

The controller is available either as a complete board, as a kit of parts or as a bare PCB, monitor EPROMs being available separately if this latter option is chosen. As such, the controller forms the basis of an attractive

system for the more serious home computing enthusiast and especially those with a hardware bias.

The System

The single board controller has been artworked in such a way that it may take either a 6502 or 6809 processor, so the types of system which may be built around it fall into two categories. A 6502-based system will be similar in many ways to a system built around the original Microtan 65, although clock frequencies up to 1.5 MHz may be used which is twice the speed of the Microtan. The CBUG monitor will be used and will give

all the usual facilities of display/ modify memory, setting breakpoints, etc, plus a line assembler and disassembler. This system will also allow BASIC resident in EPROM to be added.

A 6809 based system may be run at 1MHz or 2MHz and will use a system monitor called TVBUG. Monitor facilities are similar to those in CBUG except that the line assembler/disassembler is not included but routines for booting from disc and writing MIKBUG compatible records via the serial port are. It should be noted that the single board does not include any video circuitry, so a minimum system must either include the VDU card marketed by MCS Ltd or alternatively some sort of computer terminal interfaced via the RS232 port.

*	BOOT 5 INCH DISC OPERATING SYSTEM
/	BOOT 8 INCH DISC OPERATING SYSTEM
~	USER FUNCTION
/	OPEN LAST ACCESSED MEMORY ADDRESS
B	DISPLAY/MODIFY BREAKPOINTS
C	COPY MEMORY BLOCK
D	DISPLAY MEMORY BLOCK
F	FILL MEMORY BLOCK
G	GO (EXECUTE PROGRAM)
J	JUMP TO SUBROUTINE
M	MODIFY MEMORY
N	SET NULL PAD COUNT
P	TOGGLE PRINTER OUTPUT
R	DISPLAY/MODIFY REGISTER
S	DISPLAY STACK CONTENTS
V	COMPARE MEMORY BLOCK
W	WARM START FLEX OPERATING SYSTEM
X	REMOVE BREAKPOINTS
b	BUILD S1-S9 TAPE BLOCK
l	LOAD TAPE
s	SAVE MEMORY AS TAPE FILE
v	VERIFY TAPE

Table 1. Commands available with CBUG (6502).

M	MEMORY MODIFY/EXAMINE
L	LIST MEMORY
G	GO (EXECUTE PROGRAM)
R	REGISTER MODIFY/EXAMINE
S	SINGLE STEP MODE
N	NORMAL (NON SINGLE STEP) MODE
P	PROCEED (IN SINGLE STEP MODE)
B	SET/CLEAR BREAKPOINTS
O	OFFSETT CALCULATION
C	COPY MEMORY BLOCK
BAS	BASIC COLD START
WAR	BASIC WARM START
D	DUMP TO CASSETTE TAPE
E	EXAMINE CASSETTE TAPE
F	FETCH FROM CASSETTE TAPE
T	TRANSLATE (SINGLE LINE ASSEMBLER)
I	DIS-ASSEMBLER

Table 2. Commands available with TVBUG (6809).

PARTS LIST

RESISTORS

R1	220R	only for 20mA C/L
R2	220R	only for RS232
R3	4k7	only for RS232
R4	1k0	only for RS232
R5,11,12,14	4k7	
R6	120k	only for cassette interface
R7,8	10k	only for cassette interface
R9,13	470R	only for cassette interface
R10	10k	only for 20mA C/L
RP1	4k7 SIL pack	(7 commoned)
RP2	1k0 SIL pack	(7 commoned)
RP3	10k SIL pack	(4 separate resistors)
RP4	1k0 SIL pack	(4 separate resistors)

CAPACITORS

C1,7-14	100n	
C2,15	10n	
C3	100p	
C4,6	47n	only for cassette interface
C5	100u	

DISCRETE SEMICONDUCTORS

Tr1,3	BC184*	only for RS232
Tr2	BC184*	only for cassette interface

* NOTE BC184 HAS DIFFERENT PIN OUT TO BC184L

D1	1N4001	only for serial I/O
D2	1N4001	
D3	1N4001	
XTAL 1	8.0MHz or 6.0MHz	8.0MHz for 1 or 2MHz operation 6.0MHz for 0.75 or 1.5MHz
XTAL 2	1.8432 MHz	only for serial I/O

INTEGRATED CIRCUITS

B1	6522	Always fitted for use in computer.
B2	6522	For control applications one or two 6522s may be fitted depending on application. May be replaced by 6821s as described in text. For frequencies above 1MHz use 6522A/68B21.
C1	74LS393	
C2	874LS04	
C3	LM358N	Only for cassette interface
D1	6551	Only for serial I/O. For frequencies above 1 MHz use 6551A.
D2	6809	Either D2 or D3 should be selected.
D3	6502	For frequencies above 1MHz use 68B09/6502A.
D4	75150	only required for RS232
E2	74LS244	May be replaced by wire links for single board control application (see text).
E3	74LS244	
F3	74LS139	
G3	74LS00	
H3	74LS266	
J3	74LS12	
K3	74LS10	
L3	74LS08	
M3	74LS138	
N2	74LS245	Not required for single board applications.
N3	74S288	Memory mapping PROM. Must be programmed as described in text or obtained from MCS. An alternative for simple control application is described in the text.
E1,F1,F2,H1,H2		Memory fitted as required
K1,K2,L1,L2		For 6502 computer system the minimum configuration is CBUG(2732) in E1, 6116 in F2. For 6809 computer system the minimum configuration is TVBUG(2732) in E1, 6116 in L1.

MISCELLANEOUS.
PCB; edge connector 2X32 way A+B DIN Euro-connector; IC sockets as required.

From these minimal systems, which will allow 6502 or 6809 machine code programming and may well be adequate for those whose main interest is computer hardware, many upgrade paths are available. Hundreds of K of RAM or EPROM may be added in paged memory configuration. The addition of a disc controller and disc drives allows the FLEX or OS/9 operating system to be run on the 6809 board or TANDOS on the 6502 controller. Alternatively a Z80 card is available and allows the industry standard CP/M disc operating system to be run on systems with either processor. Other options include high resolution colour graphics, sound effects, serial and parallel I/O, EPROM programmers, real time clocks etc. Table 1 and Table 2 list the commands available under CBUG and TVBUG respectively.

The Board as a Controller

Some months ago, the author started to design a minimum configuration 6809 card to control the ETI Universal EPROM programmer in a stand-alone situation. It soon became clear that this was unnecessary because a board which would do this task at a reasonable cost was already available. Admittedly the 6502/6809 single board controller was not designed for this type of application, and it could be argued that it is a waste to use a board of this complexity for a pure control function.

This would be true if the board was only available fully built, but the fact that a bare board can be obtained and populated only as required for the particular application makes it quite suitable. The cost for control applications can be further reduced by some slight circuit modifications which remove the need for some of the more expensive components. For logic designs of reasonable complexity, the cost of a minimum configuration single board controller will be less than the component cost of a design using discrete TTL devices without even considering the time and expense of PCB artwork and manufacture.

The Circuit

The object of this section, How It Works and the constructional details is to open the board up to the electronics enthusiast. The

'Iocumentation currently provided by MCS Ltd does not really do justice to the product, a circuit diagram having only just been released, and the one presented here is more comprehensive being the result of many hours tracing the circuit from a bare PCB.

The circuit consists of:
a) The processor, which may be either a 6502 or a 6809 running at a variety of clock frequencies.
b) 9 sockets which will take standard JEDEC packages, allowing 2K, 4K or 8K RAMs or EPROMs to be used depending on link selection.
c) One 6551 configured to provide TTL serial, 20mA current loop or RS232 I/O at various baud rates.
d) Two 6522 VIAs giving 40 bits of parallel I/O, 2 counter/timers and 2 shift registers, one of which controls a cassette interface. When used in a computer system these VIAs provide interfacing for a parallel keyboard and a Centronics printer. When used as a controller, a slight circuit modification allows the 6522s to be replaced by the less expensive 6821 PIAs.
e) A bipolar PROM controlling the memory mapping of the board.
f) Signal buffering and implementation of various TANBUS signals to allow the board to be used as part of a large system by means of a system motherboard.

Construction

It is not the intention of this article to duplicate the information supplied by MCS Ltd, and this will mainly cover those points not covered by the instructions which accompany the PCB or kit. The only point to make is that the task should cause no problems to anyone familiar with the fundamentals of electronic construction. This section will cover the programming of the address decoding PROM and the ways in which the board may be modified slightly to reduce the cost of a minimum configuration system for control applications.

MCS Ltd supply a number of memory mapping PROMs for various applications but do not give instructions on how to work out the programming required to achieve a specific mapping configuration. The 74S288 PROM has a capacity of 32 bytes and, in this application, each of these bytes controls the memory configuration of a 2K block of addressing space within the 64K map. In other words, the first byte affects 0-2K

74S288 PIN No.	74S288 BIT No.	FUNCTION
9	7	A 0 IN THIS BIT ENABLES MEMORY SOCKETS 1-8. THIS IS FURTHER DECODED BY BITS 4,5 & 6.
7	6	WHEREVER A 0 OCCURS IN BIT 7 A THREE BIT BINARY NUMBER SHOULD BE WRITTEN TO THESE BITS TO INDICATE WHICH OF THE EIGHT SOCKETS IS TO BE ADDRESSED. THE SOCKET NUMBER = 1 + THE THREE BIT NUMBER e.g. 000 ADDRESSES SOCKET No.1.
6	5	
5	4	
4	3	A 0 IN THIS BIT ENABLES MEMORY SOCKET No.0. THIS IS A SPECIAL SOCKET UNAFFECTED BY CLOCK ENABLE etc. AND IS USED FOR THE MONITOR EPROM.
3	2	WHEREVER A 0 OCCURS IN BIT 7 ONE OF THESE TWO BITS SHOULD BE SET TO INDICATE WHETHER THE MEMORY SOCKET SPECIFIED BY BITS 4,5 & 6 IS TO BE CONSIDERED AS RAM OR EPROM FOR BLOCK ENABLING AND MEMORY INHIBITING PURPOSES. BIT 2 = 1 FOR RAM BIT 1 = 1 FOR EPROM
2	1	
1	0	A1 IN THIS BIT ENABLES THE TOP HALF OF THE 2K BLOCK TO BE THE I/O AREA

Table 3. Memory mapping PROM bit designations.

(0000-07FF), the second byte 2K-4K (0800-0FF) etc.

Table 3 shows the significance of each bit within these bytes, bit 0 in this illustration being the least significant and bit 7 the most significant. As an example, Table 4

shows the programming of the standard memory map PROM for a 6502 CBUG system. Looking at the bit 7 column it is clear that the sockets 1-8 are enabled for addresses 0000-2000 and C000-EFFF, these blocks being the only ones where a 0 is programmed. The columns for bits 4, 5 and 6 indicate that sockets 1, 2, 3, 4, 7 and 8 are configured for 2K devices as each of these sockets is addressed for only a single 2K block and sockets 5 and 6 are addressed for 2 blocks each and are therefore 4K devices. It can be seen that 0000-07FF addresses socket 1, 0800-0FFF — socket 2, 1000-17FF — socket 3 up to E800-EFFF — socket 8.

By looking at the bit 1 and 2 columns we can see that, of these 8 sockets, the first four have a 1 for bit 2 and are therefore RAMs and the second four have a 1 for bit 1 and are therefore EPROMs. The last two 2K blocks have a 0 in bit 3 which selects socket 0, the monitor EPROM which is obviously a 4K device, and to complete the map, a 1 in bit 0 for the block B800-BFFF indicates that the I/O area is in the top half of this block ie BC00-BFFF.

ADDRESS BLOCK	EPROM ADDRESS	DATA BITS								HEX
		7	6	5	4	3	2	1	0	
0000-07FF	00	0	0	0	0	1	1	0	0	0C
0800-0FFF	01	0	0	0	1	1	1	0	0	1C
1000-17FF	02	0	0	1	0	1	1	0	0	2C
1800-1FFF	03	0	0	1	1	1	1	0	0	3C
2000-27FF	04	1	0	0	0	1	0	0	0	88
2800-2FFF	05	1	0	0	0	1	0	0	0	88
3000-37FF	06	1	0	0	0	1	0	0	0	88
3800-3FFF	07	1	0	0	0	1	0	0	0	88
4000-47FF	08	1	0	0	0	1	0	0	0	88
4800-4FFF	09	1	0	0	0	1	0	0	0	88
5000-57FF	0A	1	0	0	0	1	0	0	0	88
5800-5FFF	0B	1	0	0	0	1	0	0	0	88
6000-67FF	0C	1	0	0	0	1	0	0	0	88
6800-6FFF	0D	1	0	0	0	1	0	0	0	88
7000-77FF	0E	1	0	0	0	1	0	0	0	88
7800-7FFF	0F	1	0	0	0	1	0	0	0	88
8000-87FF	10	1	0	0	0	1	0	0	0	88
8800-8FFF	11	1	0	0	0	1	0	0	0	88
9000-97FF	12	1	0	0	0	1	0	0	0	88
9800-9FFF	13	1	0	0	0	1	0	0	0	88
A000-A7FF	14	1	0	0	0	1	0	0	0	88
A800-AFFF	15	1	0	0	0	1	0	0	1	88
B000-B7FF	16	1	0	0	0	1	0	0	0	88
B800-BFFF	17	1	0	0	0	1	0	0	1	89
C000-C7FF	18	0	1	0	0	1	0	1	0	4A
C800-CFFF	19	0	1	0	0	1	0	1	0	4A
D000-D7FF	1A	0	1	0	1	1	0	1	0	5A
D800-DFFF	1B	0	1	0	1	1	0	1	0	5A
E000-E7FF	1C	0	1	1	0	1	0	1	0	6A
E800-EFFF	1D	0	1	1	1	1	0	1	0	7A
F000-F7FF	1E	1	0	0	0	0	0	1	0	82
F800-FFFF	1F	1	0	0	0	0	0	1	0	82

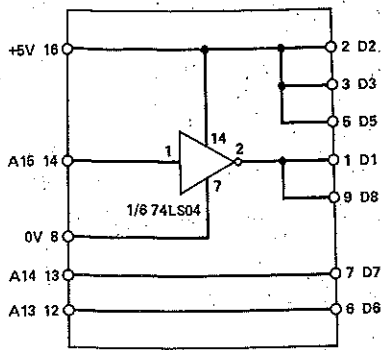Table 4. Memory mapping PROM for 6502 CBUG configuration.

Fig. 2 The circuit which may be used for memory mapping instead of a PROM in control applications.

From the foregoing information it should be clear that virtually any memory map in 2K steps can be specified by the programming of the PROM. However, for a minimal configuration as used for control applications, a cost reduction can be made by replacing this component with a number of wire links and a simple TTL device which could be soldered onto a DIL header and inserted into the PROM socket. Figure 2 shows the circuit diagram of such an arrangement which gives a crude but effective memory map for many control applications. In this map the I/O area repeats sixteen times in 2K steps starting at 0400-07FF: socket 5 is addressed at 8000-9FFF, socket 6 at A000-BFFF, socket 7 at C000-DFFF and socket 8 at E000-FFFF. Obviously if 4K devices are used they will repeat twice within the 8K block and 2K devices will repeat four times. It should be noted that this configuration does not give RAM at address 0 and accordingly will be more practical for a 6809 application than for the 6503 which generally requires zero page memory at this address.

The memory mapping PROM does not dictate the mapping of the various I/O devices within the I/O area. This is partially fixed by the hardware and partially a function of LK10, LK11, LK12 and LK13, only one of which will be fit-ted. Table 5 shows the I/O memory map.

When used as the basis of a computer system the 6522 VIAs will be required as their facilities are made use of by the system software, but in many control applications all that is required is the parallel I/O capability so the less expensive 6821 PIAs could be used. Unfortunately the pin-outs of the two devices are not identical, which means that a few tracks need cutting and few wire links require adding to the back of the board. Figure 3 shows the details of this modification. The 6821 only occupies an addressing space of 4 compared to the 16 bytes of the 6522 which means that, once the modification has been carried out, the 6821 registers will be spaced at intervals of 4 bytes. This need present no problem so long as it is not overlooked when writing the firmware.

To achieve further cost reductions for control applications it is merely necessary to omit those components which are not required for the particular application. One RAM and one EPROM will obviously be required as will at least one of the 6522 VIAs (or 681 PIAs). If no RS232 facility is required then D1, D4, Tr1, Tr3, X2 and their associated passive components may be left out. If the cassette interface is not to be used C3 and Tr2 together with their passive components can be omitted. As a final cost reducing exercise, assuming that no other boards are to be connected to the bus, the address and data bus buffers may be omitted. The data bus buffer N2 may be simply left out, but the address bus buffers E2 and E3 will require linking across as they supply on-board as well as off-board devices. This linking is done by omitting the chips in question and linking each input to its corresponding output, as may be seen from the circuit diagram (ie pins 13 to 7; 17 to 3, etc).
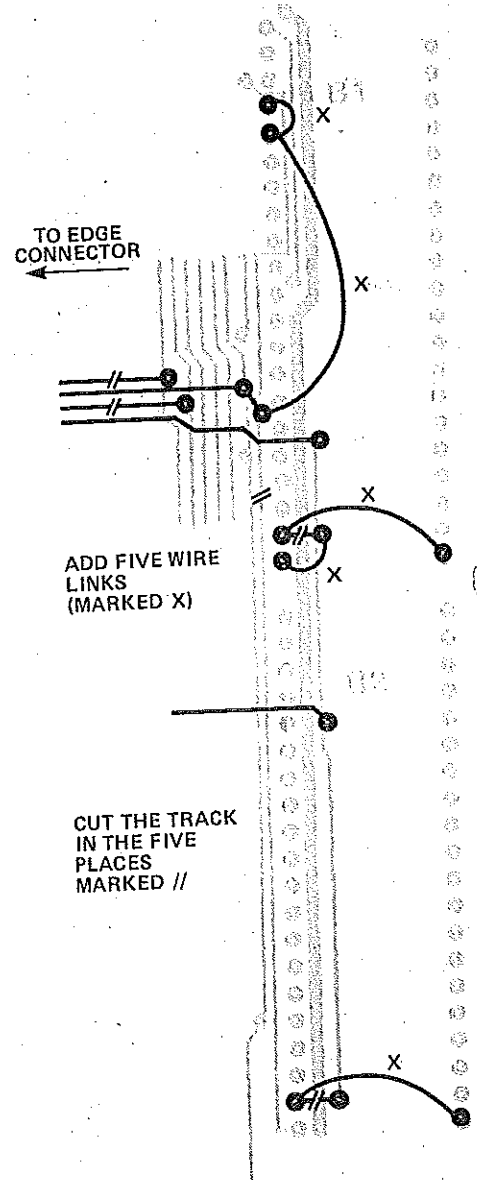
ETI

TO EDGE
CONNECTOR

ADD FIVE WIRE
LINKS
(MARKED X)

CUT THE TRACK
IN THE FIVE
PLACES
MARKED //

Fig. 3 PCB modification to enable 6821s to be used in place of 6522s.

LINK FITTED	6522 B1	START ADDRESS 6551 D1	6522 B2
LK10	I/O+00H+00H	I/O+00H+10H	I/O+00H+20H
LK11	I/O+40H+00H	I/O+40H+10H	I/O+40H+20H
LK12	I/O+80H+00H	I/O+80H+10H	I/O+80H+20H
LK13	I/O+C0H+00H	I/O+C0H+10H	I/O+C0H+20H

Table 5. Memory map of I/O area.