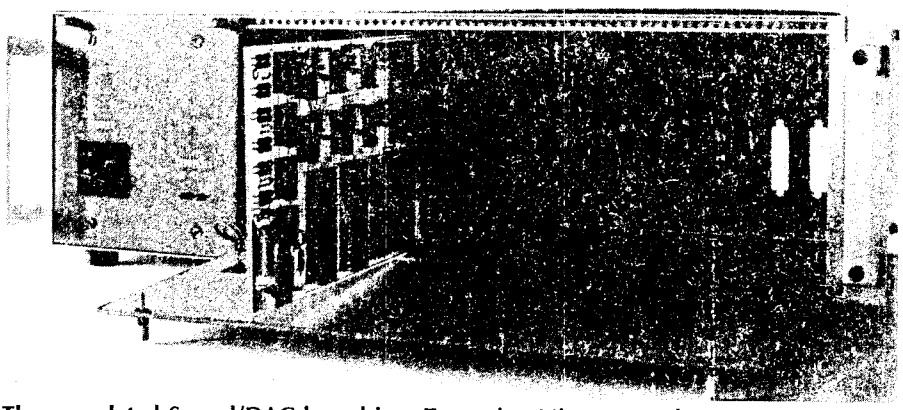
6502-BASED AUDIO BOARD

Here's a powerful and versatile peripheral for people requiring a digital-to-analogue or sound-generating capability for their computer. Although the PCB is designed for Tangerine users, the circuit may be readily interfaced to any 6502-based system. Design and development by M. D. Bedford.

When control applications on a microcomputer are proposed, it soon becomes evident that DACs and ADCs are required to interface to the real world. For more light-hearted uses and for games, the addition of sound effects can do much to enhance a program. Although multiplexed ADCs are available, giving eight or 16 channels and requiring only one eight-bit port plus control lines to support them (see the ZX ADC in the January '83 issue), DACs require eight bits per channel and would quickly use up the available I/O ports on most systems. For this reason, the circuit which is presented here was designed so that it wouldn't use system I/O ports. The board presented here is specifically intended for the Tangerine Microtan system and as such will plug directly into any expansion slot on the system motherboard: DIL switches or links are provided on the board in order to configure it to start at any 16-byte boundary within the 1K I/O area.

For users with other 6502-based systems it should not prove difficult to interface the circuit. The only non-standard signal is the one designated IO which is used in the Microtan system to indicate that an address within the I/O area (ie within the address range BC00 to BFFF) is being accessed. On any other system, address lines A10-A15 should be decoded to generate such a signal and Fig. 3 shows a simple circuit which may be used:



The completed Sound/DAC board in a Tangerine Microtan rack-mounted system. The board may be used with other 6502-based systems.

The Circuit

The DAC0800 is a low-cost high-speed multiplying DAC with an accuracy of ± 1 LSB which, when used in conjunction with an op-amp, is capable of giving a low impedance voltage output. Six of these devices have been used with 747 dual op-amps to give outputs in the range 0-10 V.

The General Instruments AY-3-8910 programmable sound generator IC forms the basis of the sound effect feature of this board, the LM380 being provided in order that a loudspeaker may be driven with no external circuitry. 6520 PIOs are used as a simple and inexpensive means of interfacing the DAC0800 and AY-3-8910, but 6821s may also be used. Buffering of some signals limits the load presented to the bus signals.

The circuitry comprising IC16, IC17 and the bank of DIL switches allows the positioning of the board in any 16-byte block within the I/O area. The start address is calculated as the binary number given by the six switches multiplied by 16, where the switches on the circuit diagram are shown in the '1' position and SW1 is the least significant. For example, if switches SW1-6 are in positions 0,0,0,0,0,1 then the first address on the board will be 16 bytes from the start of the I/O area

Construction

The layout of a printed circuit board is presented here and, due to the fairly high packing density it is suggested that, for those intending to incorporate the circuit into a Microtan system, this layout be adhered to. It should be noted that the board is of the double-sided, pinned-through type with the result that every hole not intended for the mounting of components should be fitted with a pin and soldered both on the top and the bottom of the board. Scrutiny of the overlay will reveal that this must be carried out prior to the fitting of any DIL sockets. If, however, it is not intended to fit the circuit board into a card frame along with other Tangerine boards, then a larger board may be used and some form of breadboarding technique employed for construction. If this option is taken care should be

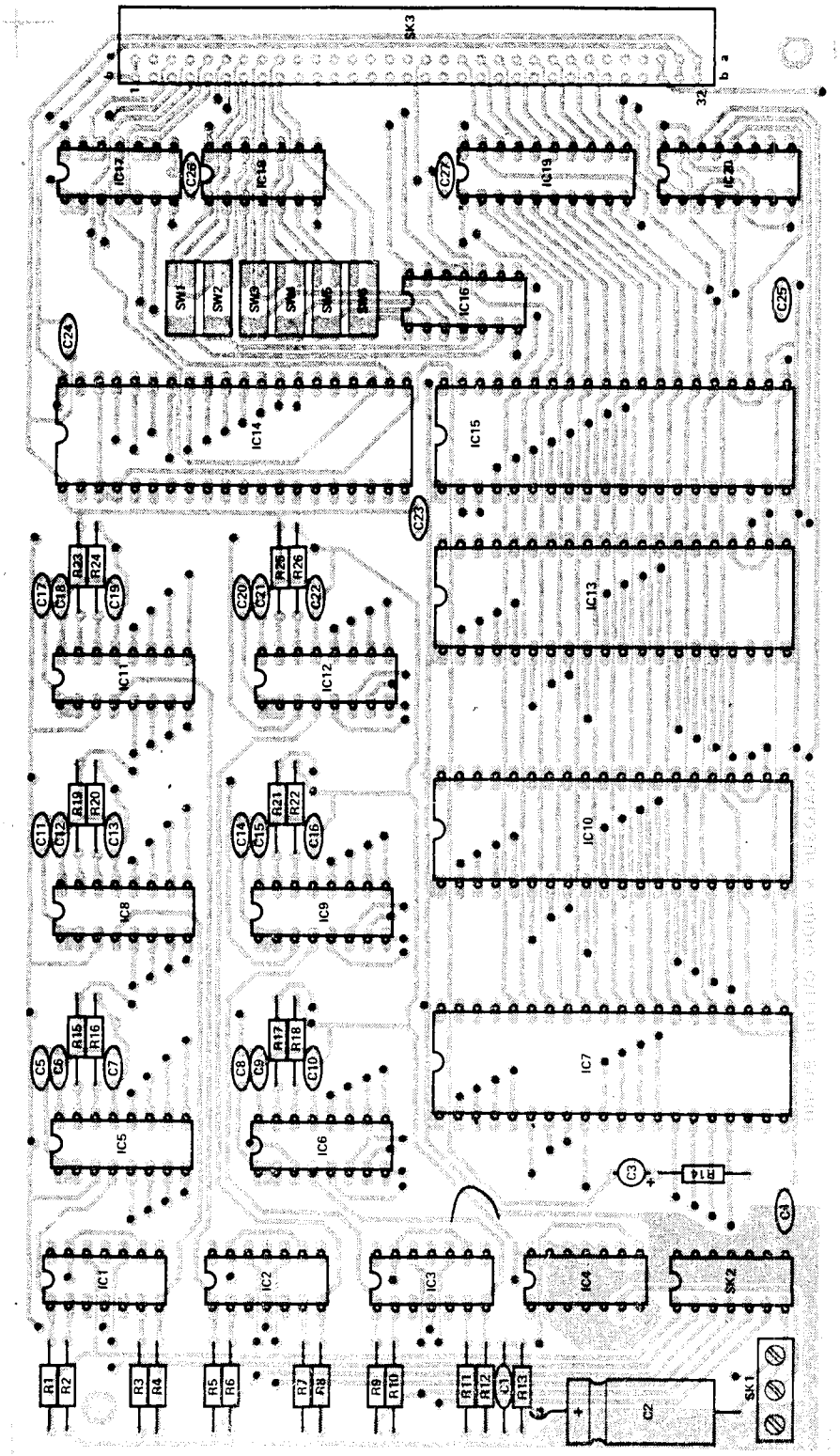


Fig. 1 Component overlay. The tinted tracks are the underside of the double-sided board: through-board pins soldered on both sides are required wherever a dot appears.

exercised in the positioning of certain capacitors. C4 and C23-27 should, as far as possible, be well distributed around the board. C7,10,13,16,19 and 22 decouple the −12 V rail, and these components should be positioned so that one capacitor from each of the two sets is close to each of the DAC0800s.

One final point applies irrespective of the method of construction: since DIL switches are relatively expensive and in such an application will most probably be set up once and rarely changed, it is suggested that, as an alternative, DIL headers with appropriate soldered links are used and plugged into DIL sockets.

PARTS LIST

Resistors (all ¼W, 5% except where stated)	
R1-12	10k 2%
R13	2R7
R14	20k
R15-26	12k 2%
Potentiometer	
RV1	22k logarithmic
Capacitors	
C1, 5, 7, 8, 10, 11, 13, 14, 16, 17, 18, 20, 21	100n ceramic
C2	470u 16 V axial electrolytic
C3	2u2 10 V tantalum
C4, 6, 9, 12, 18, 19, 22-27	10n ceramic
Semiconductors	
IC1-3	LM747
IC4	LM380
IC5, 6, 8, 9, 11, 12	DAC0800 or DAC0801
IC7, 10, 13, 15	6520, 6820 or 6821
IC14	AY-3-8910
IC16	74LS30
IC17	74LS08
IC18	74LS04
IC19	74LS245
IC20	74LS138
Miscellaneous	
SK1	3-way, 5mm pitch, PCB terminal block
SK2	14-pin DIL socket
SK3	2 × 32 way A + B DIN Euro connector (male, angled pins)
SW1-6	hex DIL changeover switch (see text)
PCB (see Buylines); DIL sockets to suit	

BUYLINES

No problems with the semiconductors for this project — it's all standard stuff and people like Technomatic, Watford and Cricklewood should have no trouble supplying you. The only difficulty may lie in finding a supplier for the DAC0800 which seems to be a bit elusive: Maplin supply the 0801 which is an acceptable substitute. The Euro socket required for Tangerine rack owners is available from Watford, while the PCB can be obtained from our PCB Service as usual. The order form is on page 83.

Programming

While it is beyond the scope of this article to give a detailed functional description of the 6520 and AY-3-8910 ICs, it is expected that the BASIC routines presented here will enable the board to be used without difficulty. In order to make full use of the sound generator, however, it is suggested that an AY-3-8910 data sheet is consulted (the company you buy the chip from should be able to help). In the routines given, the

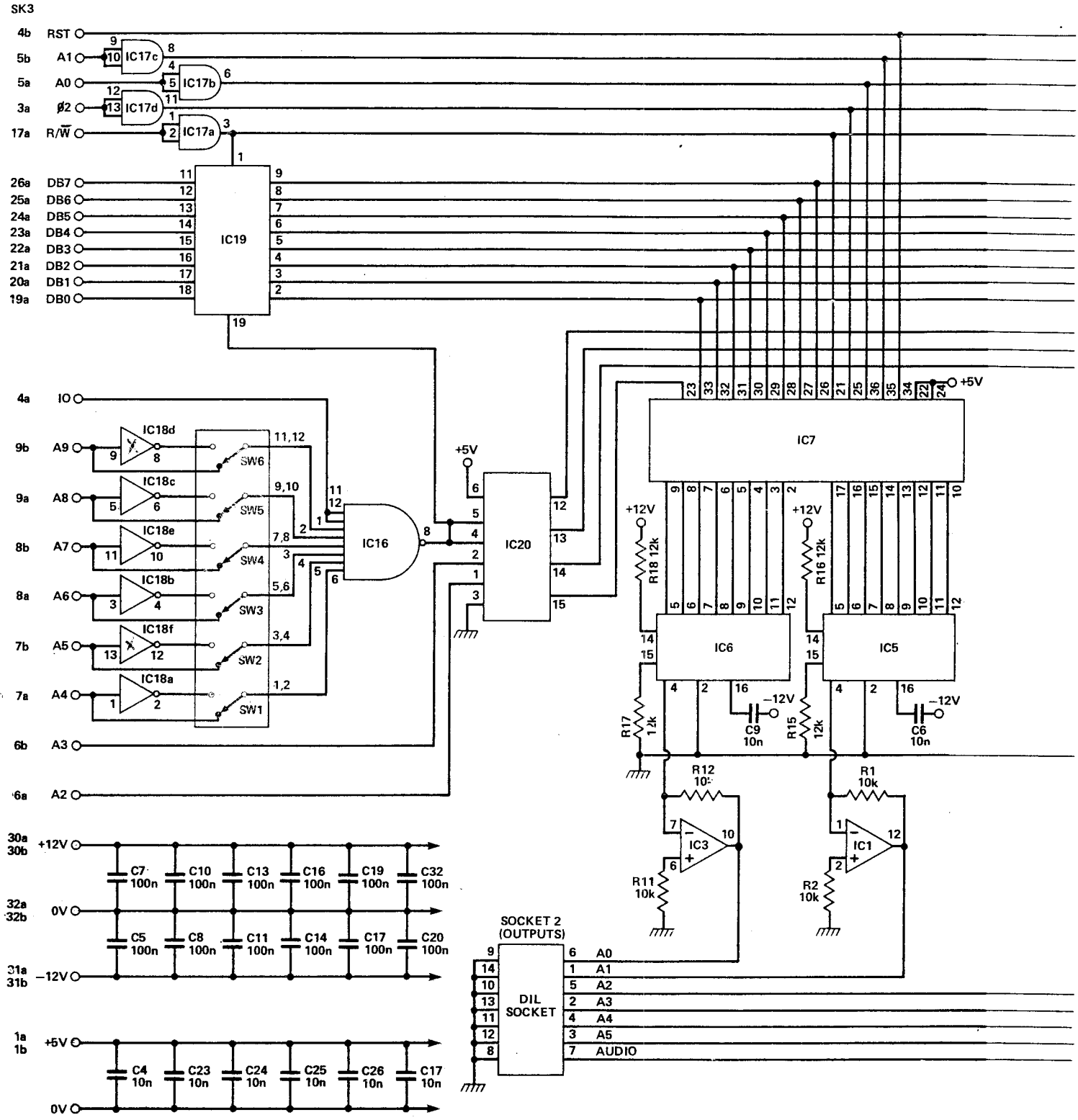


Fig. 2 Circuit diagram of the sound/DAC card.

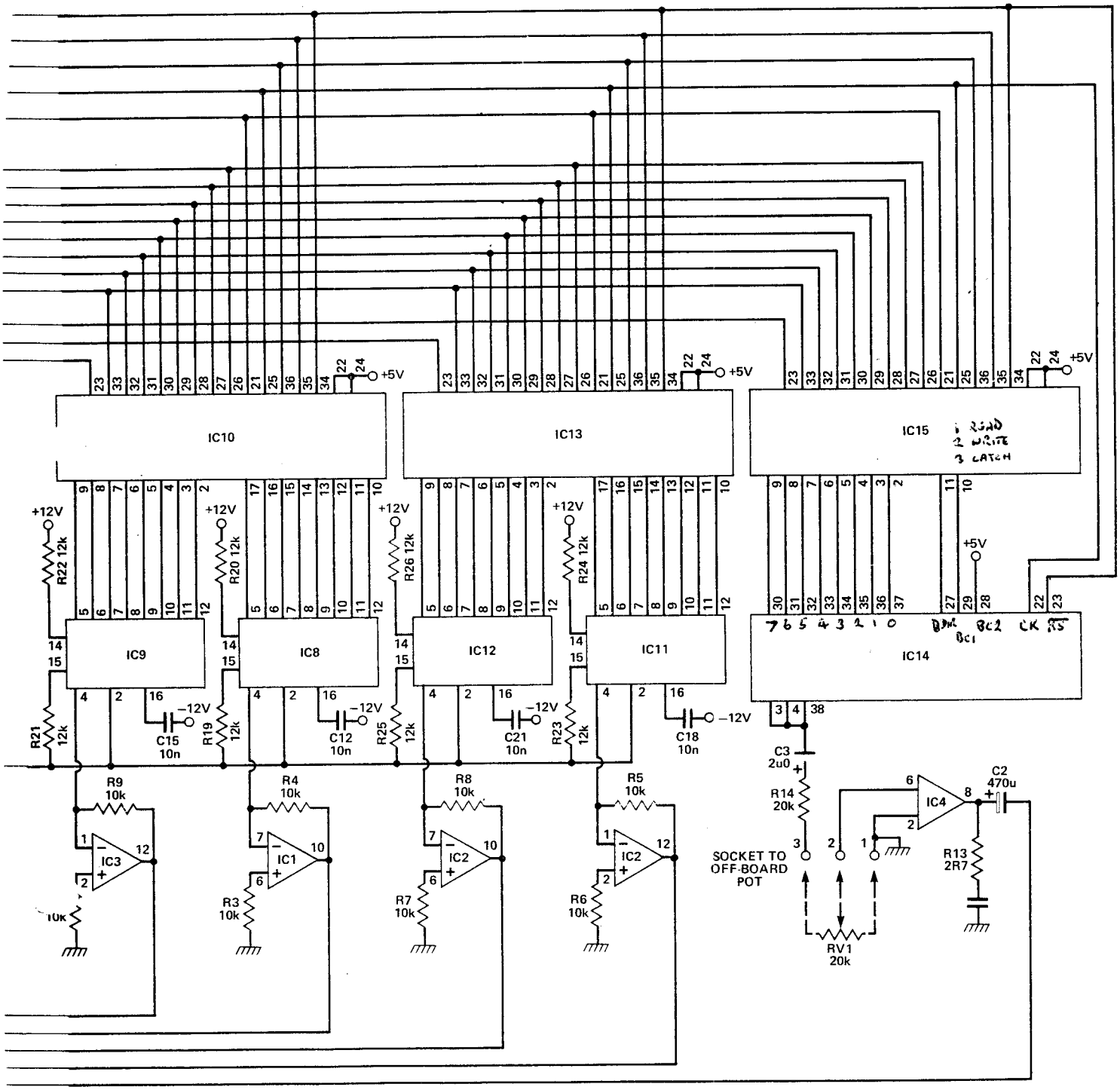
HOW I

The circuitry consists of six DACs, ICs 5-12, and one sound generator chip, IC14, which has three separate sound channels and a noise generator.

The circuitry for each of the DAC ICs is identical and we will only discuss IC6. The eight bits of data are held on pins 5-12, while the complementary current outputs are on pins 2 and 4. The DAC is configured for positive low impedance output operation, with I_{OUT} on pin 2 connected to ground and the other output fed into the buffer op-amp IC3a.

The data input to IC6 is latched by port A of the peripheral interface adapter IC7 (port B of IC7 latches the data for IC5). Similarly ICs 10 and 13 latch the data for ICs 8,9 and 11,12 respectively.

The fourth PIA, IC15, utilises both ports to control the sound generator chip, IC14. The three audio outputs of



WORKS

this chip are fed via C3, R14 and the volume control RV1 into IC audio power amp IC4. C1 and R13 form the Zobel network and C2 the DC-blocking capacitor for the amp output. The audio signal and analogue voltages are fed off-board via SK2, a DIN socket with a header plug.

Address decoding for the board is performed by ICs 16, 18 and 20. SW1-6 select which 16-byte block of memory the board occupies. For people using systems other than the Microtan, which generates the IO signal required, the additional decoding circuit for lines A10-15 shown in Fig. 3 will be required. The data bus is buffered by IC19, with the R/W signal on pin 1 selecting the direction and the output of IC16 enabling the tri-state buffers via pin 19. Bus signals which are required by several chips in the circuit are buffered by IC17.

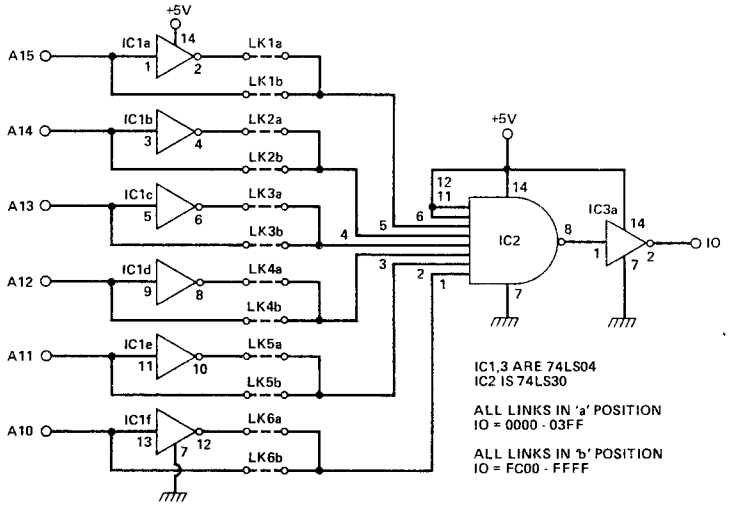


Fig. 3 Non-Microtan users who wish to build this project will require this circuit to produce the IO signal.

	IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8	IC9	IC10	IC11	IC12	IC13	IC14	IC15	IC16	IC17	IC18	IC19	IC20
0V				3,4,5 7,10 11,12			1			1			1	1	1	7	7	7	10	8
+5V							20			20			20	40	20	14	14	14	20	16
+12V	9,13	9,13	9,13	14	13	13		13	13		13	13								
−12V	4	4	4		3	3		3	3		3	3								

Table 1 This is a list of power supply connections to the various ICs for people doing their own board layout.

variable BA should be set to the base address of the board.

DAC Handling Routine. In this routine, which should be executed once at the start of the program, N should be set to the number of DAC channels to be initialised. After execution of the routine, the statement:

POKE X, BA+2*(N−1)

will write the value X to the Nth DAC channel.

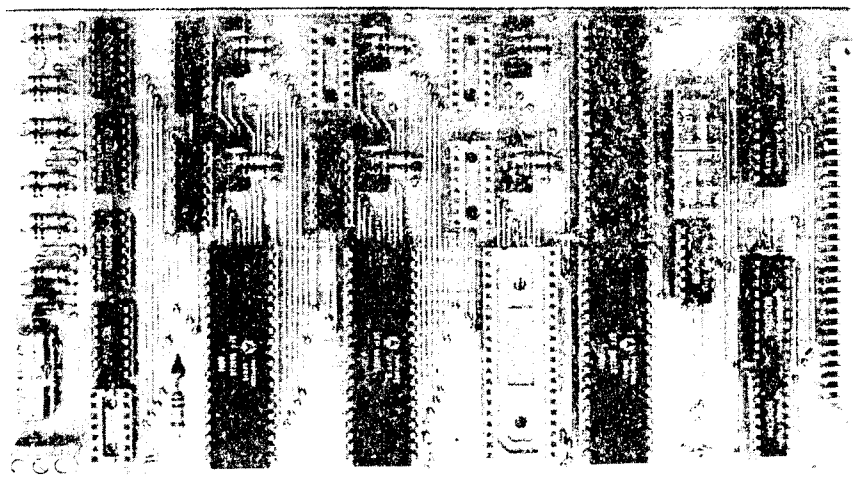
```
10 REM ....DAC INITIALISATION
20 FOR AD = BA TO BA + 2*
(N−1) STEP2
30 POKE AD+1,0: REM....ALLOW
ACCESS TO DDR
40 POKE AD,255: REM....SET DDR
TO OUTPUTS
POKE AD+1,4: REM....ALLOW
ACCESS TO OUTPUT REGISTER
60 NEXT AD
```

Sound Effect Routines. The initialisation routine should be executed once at the start of the program: after this subroutines 1000 and 2000 may be called for writes and reads respectively to the AY-3-8910 registers. In these two routines, REG should be set to the register number before entry: for a write, DAT should be set to the value of the data to be written and when reading, DAT will contain the data read after return from the subroutine.

```
10 REM....AY-3-8910
INITIALISATION
20 POKE BA+15,0: REM....6520
PORT B TO WRITE
30 POKE BA+14,255
40 POKE BA+15,4

1000 REM....AY-3-8910 WRITE
ROUTINE
1010 GOSUB 3000: REM....LATCH
ADDRESS
1020 POKE BA+12,DAT:
REM....WRITE DATA
1030 POKE BA+14,2
1040 POKE BA+14,0
1050 RETURN

2000 REM....AY-3-8910 READ
ROUTINE
2010 GOSUB 3000: REM....LATCH
ADDRESS
2020 POKE BA+13,0: REM....6520
PORT A TO READ
2030 POKE BA+12,0
2040 POKE BA+13,4
2050 POKE BA+14,1: REM....READ
DATA
2060 DAT=PEEK(BA+12)
2070 POKE BA+14,0
2080 RETURN

3000 REM .. LATCH ADDRESS
ROUTINE
3010 POKE BA+13,0: REM....6520
PORT A TO WRITE
3020 POKE BA+12,255
3030 POKE BA+13,4
3040 POKE BA+12,REG:
REM....LATCH ADDRESS
3050 POKE BA+14,3
3060 POKE BA+14,0
3070 RETURN
```

Where it is only intended to write to the AY-3-8910 registers, a saving in execution time and program size may be made by incorporating lines 3010-3030 of the latch address routine into the initialisation routine and using the following routine for writing. In this case subroutines 2000 and 3000 are not required.

```
1000 REM....AY-3-8910 WRITE
ROUTINE FOR WRITE-ONLY
APPLICATIONS
1010 POKE BA+12,REG:
REM....LATCH ADDRESS
1020 POKE BA+14,3
1030 POKE BA+14,0
1040 POKE BA+12,DAT:
REM....WRITE DATA
1050 POKE BA+14,2
1060 POKE BA+14,0
1070 RETURN
```



A completed board, sporting the sound chip and three of the possible six DAC channels.